

CAST

PCI-M64AHB

64-bit/66MHz PCI to AMBA AHB Interface Core

Features

- PCI specification 2.3 compliant
- 66MHz PCI performance
- 64-bit PCI data path
- Zero wait states burst mode
- Full PCI bus master/target functionality
- Single PCI interrupt support
- Type 0 PCI Configuration space
- PCI Parity generation and parity error detection.
- PCI-AHB window size from 16B to 2GB
- 64-bit DMA Controller
- Eight 64-bit Mailboxes
- AHB bus interrupt
- Available in synthesizable HDL source code
- Verified in Xilinx Virtex-II FPGA

The main purpose of the PCI-M64AHB Core is to act as a simple bridge between the PCI bus and the AMBA AHB bus.

The PCI-M64AHB Interface supports a 64-bit address/data bus and operates at up to a 66MHz PCI clock frequency. It is fully compliant with the PCI Local Bus Specification, Revision 2.3. The PCI-M64AHB core can be used in ASIC and FPGA devices.

The interface implements 64 bytes of PCI Configuration Space registers. It is possible to extend the Configuration Space up to 256 bytes for application needs.

The core allows PCI-AHB transfers and DMA data transfers in both directions.

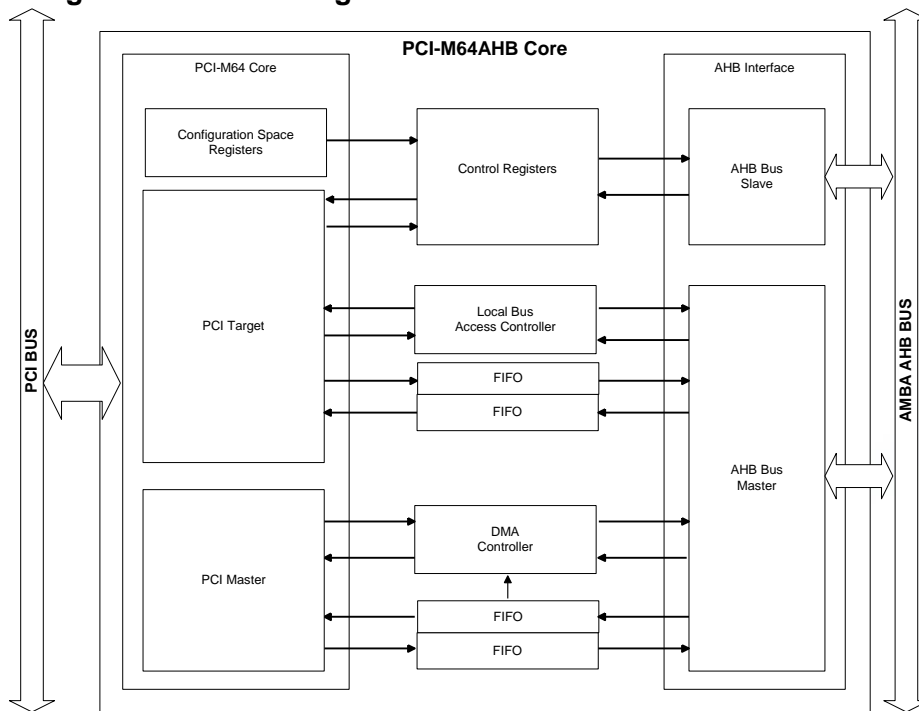
The PCI-AHB transfer window can range from 16 bytes to 2GB.

Applications

The PCI-M64AHB can be utilized for a variety of PCI Interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

Bridge Architecture Diagram



Functional Description

As shown above and explained below, the PCI-M64AHB includes six major blocks: Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Target State Machine, and Master State Machine.

PCI-M64 Core

The PCI-M64 core controls access to the PCI bus. The PCI-M64 core can be divided to three major subsystems – PCI Target controller, PCI Master controller and Configuration Space register.

Target Access Controller

The target access controller handles transactions from the PCI bus to the AHB memory space initiated by a device on the PCI bus.

DMA Controller

The DMA Controller allows efficient high-speed data transfers between the PCI address space and the AHB address space.

Control Registers

The Control Registers control core functionality including DMA channel, PCI-AHB window, and interrupts. The control register block includes PCI and AHB mailboxes.

AHB Bus Slave

The AHB Bus Slave allows devices on the AHB bus to access core control registers.

AHB Bus Master

The AHB Bus Master performs data transfers on the AHB bus.

Implementation Results

PCI-M64AHB reference designs have been evaluated in a variety of technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench including vectors and expected results
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide