

CAST



PCI-M64

64-bit/66Mhz PCI Master/Target Interface Core

The PCI-M64 core provides a fast, fully-featured, master/target interface that complies with the PCI Local Bus Specification, Rev. 2.3.

It supports a 64-bit address/data bus and operates at up to 66 MHz PCI clock frequency. The 64-byte Configuration Space is extendible to 256 bytes. The Target function supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 2 GB.

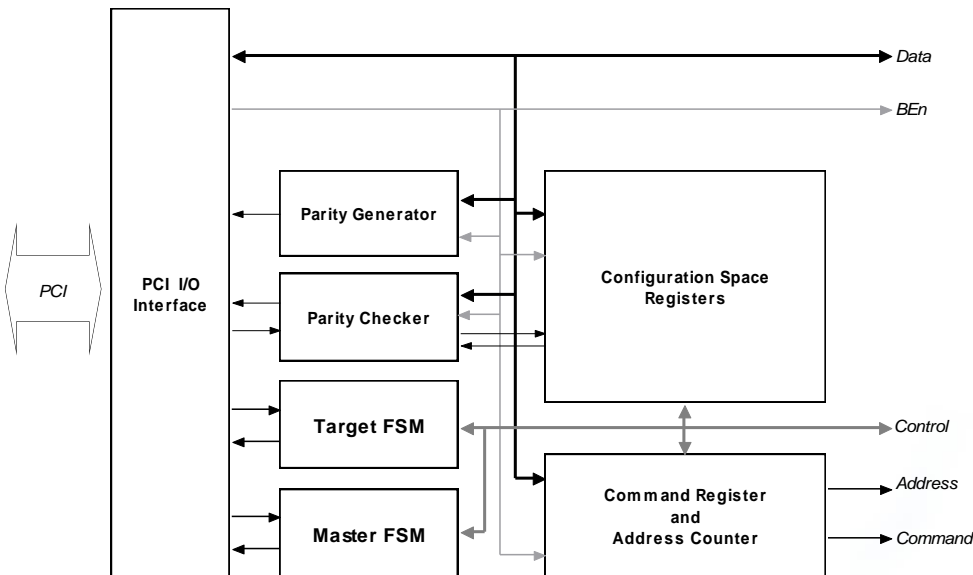
The PCI-M64 is designed for reuse in ASIC or FPGA implementations.

Applications

The PCI-M64 can be utilized for a variety of PCI Interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

PCI Interface Architecture Diagram



Features

- Compliant with PCI Local Bus Specification, Revision 2.3
- 66 MHz performance (PCI clock frequency)
- 64-bit datapath
- Zero wait states burst mode
- Full bus Master/Target functionality
- Single interrupt support
- Type 0 Configuration space
- Implements 64 bytes of PCI Configuration Space registers; Configuration Space can be extended up to 256 bytes if required.
- Target portion supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 2 GB
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection.
- Both Target and Master supported commands are:
 - Configuration Read, Configuration Write
 - Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL)
 - I/O Read, I/O Write.
- Available in flexible HDL form for synthesis, or as an optimized netlist for various FPGA families; Verified in a Xilinx Virtex FPGA
- 64-bit DMA Controller Core supporting independent write and read operations available

Functional Description

As shown in the PCI Interface Architecture diagram, the PCI-M64 includes five major blocks: Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Target State Machine.

Parity Generator

The parity generator generates parity during read transaction.

Parity Checker

The parity checker checks parity during command phase and write transaction.

Configuration Space Registers

Configuration Space Registers block implements the mandatory 64 bytes of PCI Configuration Space registers. See the chapter PCI Configuration Space for more details.

Command Register and Address Counter block

Command Register saves a transaction command at the beginning of PCI transaction. Address Counter block generates a backend address. Address counter is controlled by the Target FSM.

Target FSM

Target State Machine is in charge of handling PCI target transactions protocol.

Master FSM

Master State Machine is in charge of initiating PCI transactions.

DMA Controller Core

The DMA Controller is a part of the PCI-M64 deliverables. The controller is optimized for direct cooperation with the PCI-M64 Interface. The controller offers independent write and read transactions and significantly reduces the complexity of the user application design. Usage of FIFOs ensures achievement of full speed burst data transfers. DMA Registers are accessible from the PCI bus using the PCI interface Target functions and can be both mapped to the I/O or Memory space.

Implementation Results

PCI-M64 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with IOBs assuming all core PCI I/Os are routed off-chip, and slices with single base address register configuration.

Supported Family	Slices	IOBs	GCLK	BRAM	Fmax (MHz)
Virtex-II XC2V1000-5	318	89	1	0	66
Virtex-II Pro XC2VP4-6	312	89	1	0	66
Virtex-4 XC2VLX15-10	318	89	1	0	66
Virtex-4 XC2VFX12-10	318	89	1	0	66
Virtex-4 XC2VFX12-10	312	89	1	0	66

Results generated with ISE 8.1.03i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist for PCI-M64 Core
- Post-synthesis EDIF netlist for DMA Controller
- Sophisticated HDL Testbench including vectors and expected results
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide