

CAST



PCI-M32MF

Multi-Function PCI Master/Target Interface Core

The PCI-M32MF implements a master/target PCI interface compliant with the PCI 2.3 specification. It supports a 32-bit address/data bus and operates up to 33 MHz (66 MHz optional) PCI clock.

The core offers one to eight independent PCI functions in a single chip, each implementing 64 to 256 bytes of PCI Configuration Space registers as required. Each function supports up to six Base Address Registers, with both I/O and Memory space decoding from 16 bytes up to 4GB.

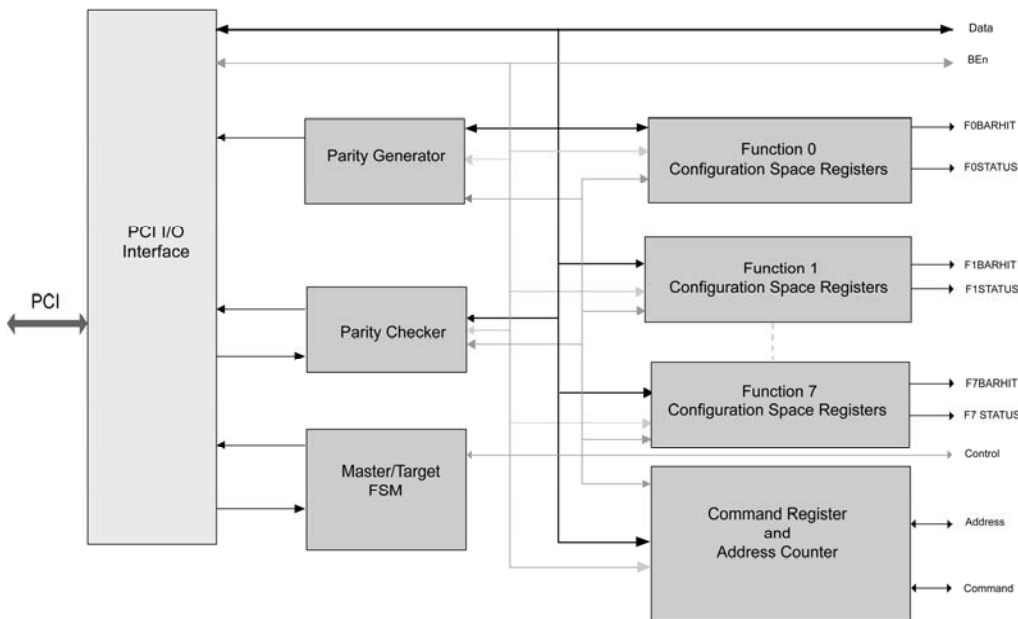
The core was developed for easy reuse with ASICs or FPGAs.

Applications

The PCI-M32MF can be utilized for a variety of PCI interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

PCI Interface Architecture Diagram



Features

- Fully compliant with the PCI Local Bus Specification, Revision 2.3.
- 33 MHz performance (66 MHz optional)
- 32-bit datapath
- Full Master/Target functionality, with support for these commands:
 - Configuration Read, Configuration Write
 - Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL), Memory Write and Invalidate (MWI)
 - I/O Read, I/O Write
- Zero wait states burst mode
- Support all interrupt pins (INTA#, INTB#, INTC#, INTD#)
- Type 0 Configuration space
- Supports all Base Address Registers
- Supports backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- Silicon-verified in FPGA

Functional Description

As shown in the PCI Interface Architecture diagram, the PCI-M32MF includes five major blocks: Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Master/Target State Machine.

Parity Generator

The parity generator generates parity during read transaction.

Parity Checker

The parity checker checks parity during command phase and write transaction.

Configuration Space Registers

The PCI-M32MF contains up to eight configuration space registers depending on the core setup. The configuration space register block implements the mandatory 64 bytes of PCI Configuration Space registers.

Command Register and Address Counter block

Command Register saves a transaction command at the beginning of PCI transaction. Address Counter block generates a backend address. Address counter is controlled by Target FSM.

Master/Target FSM

Master/Target State Machine is a control block of the PCI-M32MF interface. Target state machine is in charge of handling PCI transactions protocol. Master State Machine is in charge of initiating PCI transactions.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been implemented into a FPGA.

Implementation Results

Reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results for the following configuration: Function 0 with 2 BARs and Function 1 with 1 BAR.

Xilinx Device	Slices	BRAM	I/Os	Fmax (MHz)	ISE
Spartan-3E XC3S500E-4	577	-	53	33	10.1.03
Spartan-6 XC6SLX9-2	236	-	53	33	11.3
Virtex-4 XC4VLX15-10	567	-	53	33	10.1.03
Virtex-5 XC5VLX30-1	297	-	53	33	10.1.03

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench including vectors and expected results
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide