PCI-M32MF
32-bit / 33MHz Multi-Function PCI Master/Target Core

intel FPGA

The PCI-M32MF implements a master/target PCI interface compliant with the PCI 2.3 specification. It supports a 32-bit address/data bus and operates up to 33 MHz PCI clock.

The core offers one to eight independent PCI functions in a single chip, each implementing 64 to 256 bytes of PCI Configuration Space registers as required. Each function supports up to six Base Address Registers, with both I/O and Memory space decoding from 16 bytes up to 4GB.

The PCI- M32MF builds on more than 15 years of CAST PCI IP expertise and has been designed for straightforward reuse, with proven design practices that ensure easy integration and smooth technology mapping. The core is available in synthesizable RTL or as a targeted FPGA netlist, and is delivered with everything required for rapid and successful integration and implementation.

Applications

The PCI-M32MF can be utilized for a variety of PCI interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications
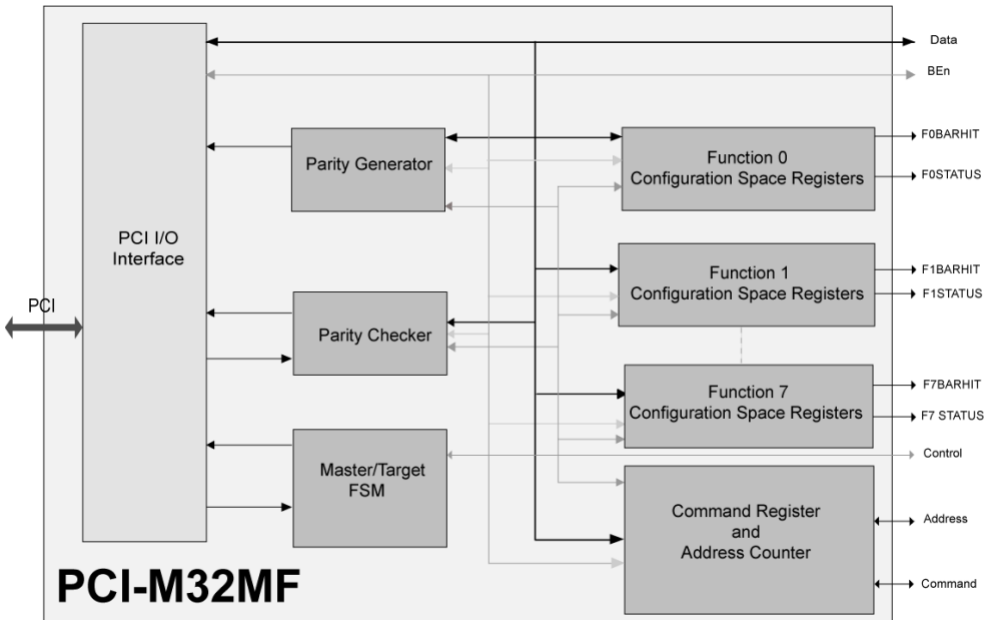
FEATURES

- Fully compliant with the PCI Local Bus Specification, Revision 2.3.
- 33 MHz performance 32-bit datapath
- Full Master/Target functionality, with support for these commands:
  - Configuration Read, Configuration Write
  - Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL), Memory Write and Invalidate (MWI)
  - I/O Read, I/O Write
- Zero wait states burst mode
- Support all interrupt pins (INTA#, INTB#, INTC#, INTD#)
- Type 0 Configuration space
- Supports all Base Address Registers
- Supports backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- Silicon-proven

Block Diagram

CAST

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

Reference designs have been evaluated in a variety of technologies. The following are sample Intel results for the following configuration: Function 0 with 2 BARs and Function 1 with 1 BAR.

Altera Device	LEs/ ALUTs	Memory	I/Os	Fmax (MHz)	Quartus
Cyclone-II EP2C5-8	925	-	53	33	8.1
Cyclone-III EP3C10-8	935	-	53	33	8.1
Stratix-II EP2S15-5	606	-	53	33	8.1
Stratix-III EP3S50-4	604	-	53	33	8.1

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been implemented into a FPGA.

Deliverables

The Core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis netlist
- Sophisticated HDL Testbench including vectors and expected results
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

CAST PCI Cores Family

CAST offers a broad family of PCI cores the members of which along with their basic features are outlined in the following table.

	PCI-T32	PCI-T32MF	PCI-M32	PCI-M32MF	PCI-HB	PCI-HB-AHB	PCI-DHB-AHB
PCI 33 MHz	✔	✔	✔	✔	✔	✔	✔
Host	✖	✖	✖	✖	✔	✔	✔
Master	✖	✖	✔	✔	✖	✖	✔
Target	✔	✔	✔	✔	✖	✖	✔
Multifunction	✖	✔	✖	✔	✖	✖	✖
32bit	✔	✔	✔	✔	✔	✔	✔
64bit	✖	✖	✖	✖	✖	✖	✖
SoC Interface	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AHB, AXI, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, Avalon-MM[1]	AHB	AHB
ASIC Support	✔	✔	✔	✔	✔	✔	✔
FPGA Support	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]

Notes:
- ✔ : Feature is supported
- ✔ : Feature optionally supported
- ✖ : Feature is not supported
- 1 : SoC interface in grey font can be made available upon request
- 2 : FPGA devices that do not support PCI I/O standard are not supported