

CAST



PCI-M32

32-bit/33MHz PCI Master/Target Interface Core

Features

- Flexible synthesizable VHDL
- PCI specification 2.3 compliant
- 33 MHz performance (66MHz optional)
- 32-bit datapath
- Zero wait states burst mode
- Full bus Master/Target functionality
- Single interrupt support
- Type 0 Configuration space
- Support of all Base Address Registers
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- Available in synthesizable VHDL source code
- DMA Controller Core supporting independent write and read operations available

The main PCI-M32 Interface core purpose is to isolate the user from having to solve complex problems of the PCI interface implementation and let the user instead focus on the application development.

The PCI-M32 Interface supports 32-bit address/data bus and operates up to 33 MHz (66 MHz optional) PCI clock frequency. It is fully compliant with the PCI Local Bus Specification, Revision 2.3.

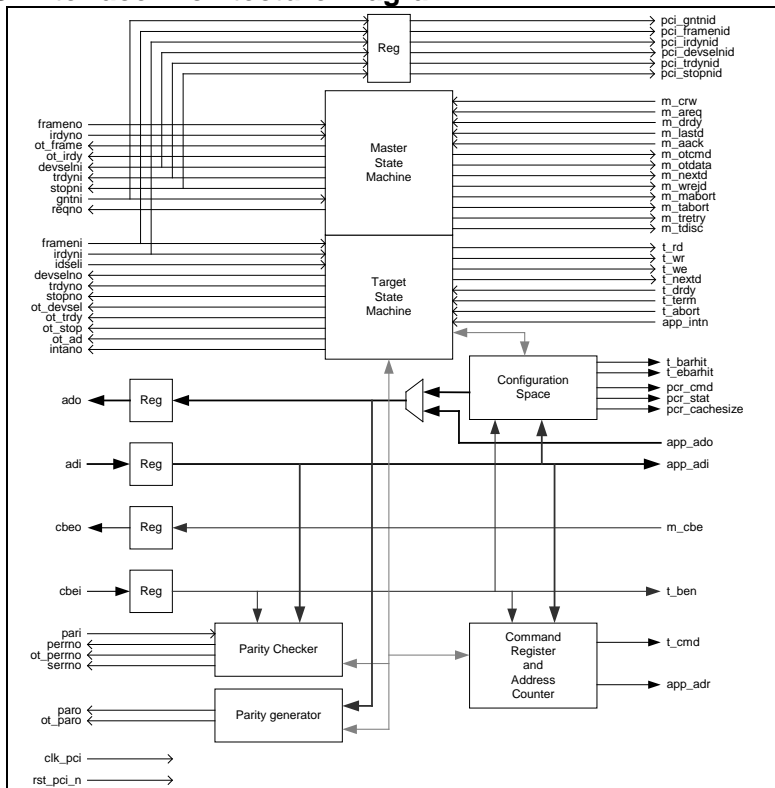
The PCI-M32 Interface has both Master and Target capabilities. The interface implements 64 bytes of PCI Configuration Space registers. It is possible to extend the Configuration Space up to 256 bytes if required.

The Target part supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 2 GB. Both Target and Master supported commands are:

- Configuration Read, Configuration Write
- Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL)
- I/O Read, I/O Write

The PCI-M32 is designed for reuse in ASIC or FPGA implementations.

PCI Interface Architecture Diagram



Applications

The PCI-M32 core can be utilized for a variety of applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

Functional Description

As shown in the PCI Interface Architecture Diagram, the PCI-M32 includes six major blocks: Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Target State Machine and Master State machine.

Parity Generator

The parity generator generates parity during read transaction.

Parity Checker

The parity checker checks parity during command phase and write transaction.

Configuration Space Registers

Configuration Space Registers block implements the mandatory 64 bytes of PCI Configuration Space registers. See the chapter PCI Configuration Space for more details.

Command Register and Address Counter block

Command Register saves a transaction command at the beginning of PCI transaction. Address Counter block generates a backend address. Address counter is controlled by the target FSM.

Target FSM

Target State Machine is in charge of handling PCI target transactions protocol.

Master FSM

Master State Machine is in charge of initiating PCI transactions.

DMA Controller Core

The DMA Controller is a part of the PCI-M32 deliverables. The controller is optimized for direct cooperation with the PCI-M32 Interface. The controller offers independent write and read transactions and significantly reduces the complexity of the user application design. Usage of FIFOs ensures achievement of full speed burst data transfers. DMA Registers are accessible from the PCI bus using the PCI interface Target functions and can be both mapped to the I/O or Memory space.

Implementation Results

PCI-M32 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with IOBs assuming all PCI only I/Os are routed off-chip, and with single base address register configuration without DMA.

Supported Family	Slices	IOBs	BRAM	Fmax (MHz)	ISE Version
Spartan-3E 3S250E-4	258	51	0	33	12.2i
Spartan-6 6SLX25-2	144	51	0	33	12.2i
Virtex-4 4V SX25-10	225	51	0	33	12.2i
Virtex-5 5VLX50-1	162	51	0	33	12.2i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist for PCI-M32 Core
- Post-synthesis EDIF netlist for DMA Controller
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide