The PCI Host Bridge core enables data transfers between a host processor system and PCI bus based devices. The bridge is in charge of PCI bus arbitration, generating PCI clock and reset signals. An important part of the bridge is the bus arbiter.

The PCI-HB core is a generic core, which provides all the essential bridge functions without a host bus interface.

Applications

The PCI-HB can be utilized in a variety of PCI Interface applications including:

- PCI-AMBA host bridge
- PCI-CoreConnect bus host bridge
- Embedded system PCI applications

PCI Host Bridge Architecture Diagram
**Functional Description**

The above shown PCI Host Bridge architecture diagram describes a full bridge, which consists of a generic PCI bridge core and user dependent parts (Target Data Interface, Dual-port memory and Host bus interface).

**Configuration Space Registers**

The Configuration Space Registers block implements the mandatory 64 bytes of the PCI Configuration Space registers. The registers can be accessible from both the PCI bus and the host bus.

**PCI Master**

The PCI master initiates PCI bus transactions. Transaction parameters are delivered from the Initiator controller.

**PCI Target**

The PCI target data interface enables access to the host address space from the PCI bus agents (cards).

**PCI Bus Arbiter**

The PCI Bus arbiter grants a PCI bus mastership to one of the bus agents. The arbiter has to grant mastership to the PCI-HB core when the bus is idle to park the bus. There are optional features, which can be implemented in the bridge:

- Different schemes of bus granting (fixed priority, adjustable priority)
- Master agent malfunction detection and reporting (bus master agent requested mastership bus does not initiate transaction when granted)

**Reset Generator**

The reset signal has to be asserted for a minimum of 1ms after power-up. The PCI specification defines that the PCI agents has to be ready to receive the first configuration transactions within $2^{25}$ PCI Clock cycles after reset.

**Interrupt Controller**

The interrupt controller monitors the PCI interrupt signals (INTx#) and the PCI system error signal (SERR#). Host interrupt assertion is controlled by an interrupt mask register.

**Bridge Control**

The bridge control block controls all the bridge functions and interrupt propagation from the PCI side to the host processor system.

**Initiator controller**

The Initiator controller is the heart of the bridge. The controller has to be able to initiate the following transactions:

- Configuration space read/write
- Memory space read/write
- I/O Space read/write
- Interrupt acknowledge (optional)
- Special cycles (optional)
Implementation Results

PCI-HB reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with IOBs assuming all PCI-HB only I/Os are routed off-chip and slices with single base address register configuration.

<table>
<thead>
<tr>
<th>Supported Family</th>
<th>Slices</th>
<th>IOBs</th>
<th>BRAM</th>
<th>Fmax (MHz)</th>
<th>ISE Version</th>
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</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide