

CAST



PCI-HB

32-bit/33, 66MHz PCI Host Bridge Core

Features

- PCI specification 2.3 compliant
- 33/66 MHz performance
- 32-bit datapath
- PCI reset generator
- PCI bus arbiter (up to 7 external bus agents)
- Interrupt controller
- Parity generation and parity error detection.
- Dual-port based shared memory
- PCI Configuration registers accessible from both PCI and host directions
- Available in synthesizable VHDL source code

The PCI Host Bridge core enables data transfers between a host processor system and PCI bus based devices. The bridge is in charge of PCI bus arbitration, generating PCI clock and reset signals. An important part of the bridge is the bus arbiter.

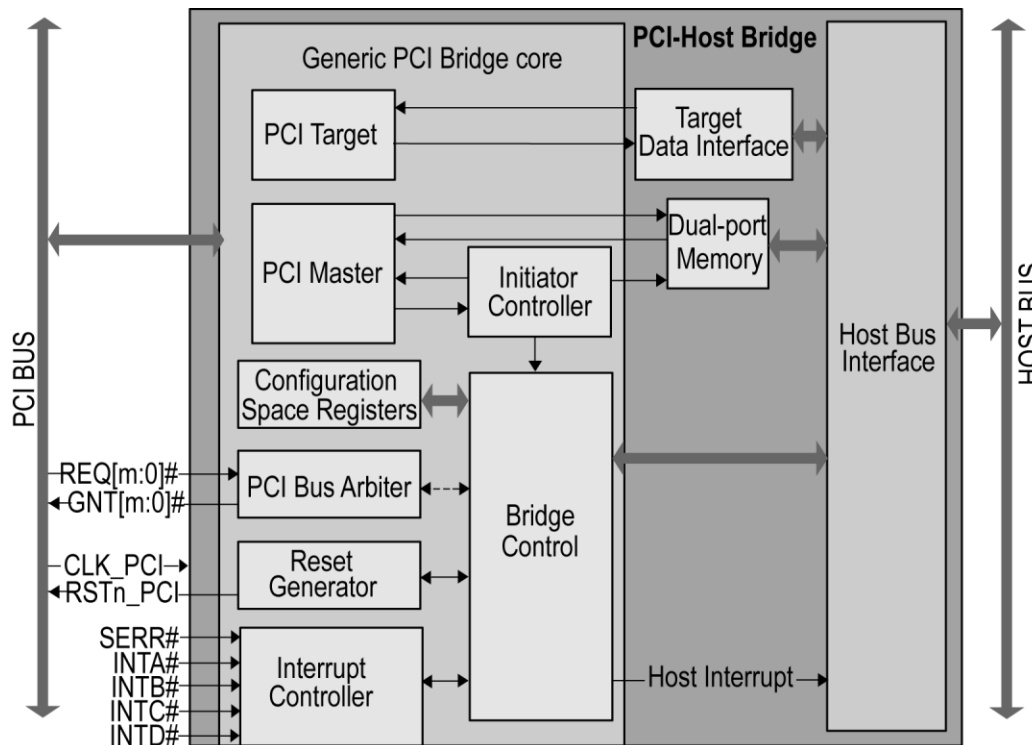
The PCI-HB core is a generic core, which provides all the essential bridge functions without a host bus interface.

Applications

The PCI-HB can be utilized in a variety of PCI Interface applications including:

- PCI-AMBA host bridge
- PCI-CoreConnect bus host bridge
- Embedded system PCI applications

PCI Host Bridge Architecture Diagram



Functional Description

The above shown PCI Host Bridge architecture diagram describes a full bridge, which consists of a generic PCI bridge core and user dependent parts (Target Data Interface, Dual-port memory and Host bus interface).

Configuration Space Registers

The Configuration Space Registers block implements the mandatory 64 bytes of the PCI Configuration Space registers. The registers can be accessible from both the PCI bus and the host bus.

PCI Master

The PCI master initiates PCI bus transactions. Transaction parameters are delivered from the Initiator controller

PCI Target

The PCI target data interface enables access to the host address space from the PCI bus agents (cards).

PCI Bus Arbiter

The PCI Bus arbiter grants a PCI bus mastership to one of the bus agents. The arbiter has to grant mastership to the PCI-HB core when the bus is idle to park the bus. There are optional features, which can be implemented in the bridge:

- Different schemes of bus granting (fixed priority, adjustable priority)
- Master agent malfunction detection and reporting (bus master agent requested mastership bus does not initiate transaction when granted)

Reset Generator

The reset signal has to be asserted for a minimum of 1ms after power-up. The PCI specification defines that the PCI agents has to be ready to receive the first configuration transactions within 2^{25} PCI Clock cycles after reset.

Interrupt Controller

The interrupt controller monitors the PCI interrupt signals (INTx#) and the PCI system error signal (SERR#). Host interrupt assertion is controlled by an interrupt mask register.

Bridge Control

The bridge control block controls all the bridge functions and interrupt propagation from the PCI side to the host processor system.

Initiator controller

The Initiator controller is the heart of the bridge. The controller has to be able to initiate the following transactions:

- Configuration space read/write
- Memory space read/write
- I/O Space read/write
- Interrupt acknowledge (optional)
- Special cycles (optional)

The controller has a set of registers which defines transaction parameters and a starting address of the data in a dual-port memory.

Target Data Interface

Provides data buffering and clock domain crossing between the PCI Target and the Host interface.

Dual-port memory

The dual-port memory is accessible from both the initiator controller and the host processor bus sides. Its implementation is technology dependent.

Host bus interface

The host interface slave allows the host processor access dual-port memories, bridge PCI configuration space registers and bridge control registers.

PCI bus arbitration

The PCI bus arbitration is controlled by a PCI bus arbiter. The arbiter supports up to eight masters. The bridge's PCI interface is internally connected to the arbiter. The arbiter uses the bridge's PCI interface core as a default PCI bus park master.

PCI bus reset

The PCI bus reset is a process where the PCI host bridge has to assert *rstno*. There are certain timing constrains for the reset process. The reset signal *rstno* has to be asserted at least 1ms after power-up. The bridge is ready to initiate the first configuration access after 2^{25} clock cycles from the reset signal deassertion. The host bridge readiness to perform PCI transactions is indicated in the bridge status register.

PCI bus clock

The PCI Host Bridge core does not contain a PCI bus clock generator since the implementation is application dependent. The PCI clock can be derived from a host clock or generated by an external clock source. The PCI bus clock has to follow PCI bus specification.

Implementation Results

PCI-HB reference designs have been evaluated in a variety of technologies. The following are sample Lattice results for the following configuration: single base address register configuration & support for 8 bus masters:

Lattice Device	LUT4s	Reg-isters	Slices	SysMEM EBRs	External I/Os	Speed (f _{max} , MHz)
LFSC3GA25E-6	1569	649	1187	-	65	33
LFE2-50E-6	1357	590	1029	-	65	33
LFEC6E-4	1417	594	1061	-	65	33
LFXP6C-4	1417	594	1061	-	65	33
LCMXO280C-4	1177	590	790	-	65	33

See the web site for other implementation results.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Lattice version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide