PCI-HB
32-bit/33MHz PCI Host Bridge
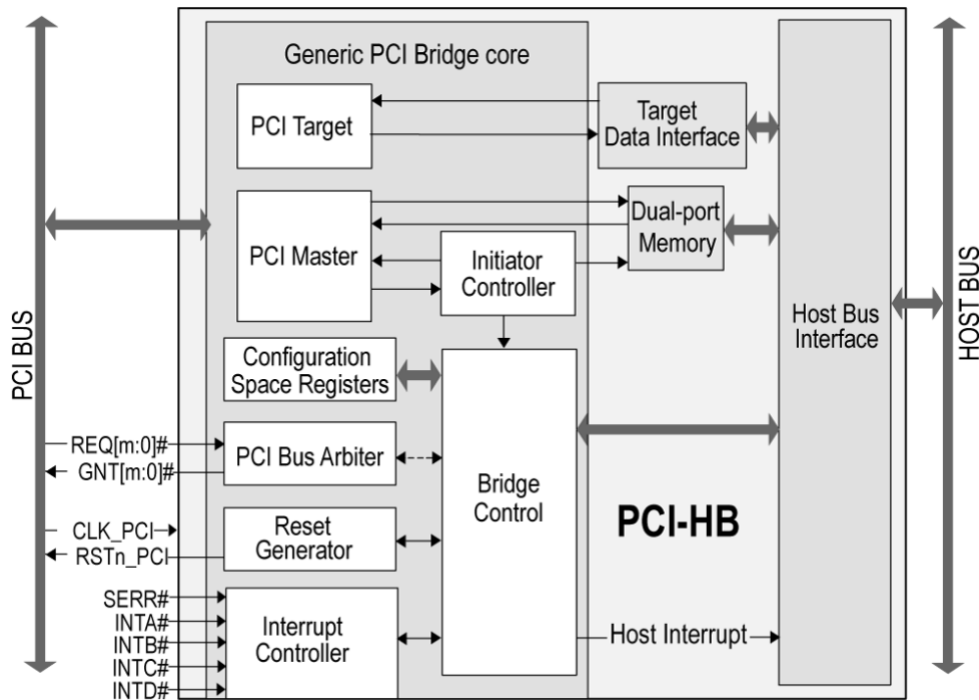
LATTICE SEMICONDUCTOR™

This PCI Host Bridge IP core enables data transfers between a host processor and PCI bus based devices.

The bridge allows the host to initiate PCI accesses or to respond to transactions initiated by other PCI devices.

The core complies with the PCI bus specification versions 3.0 and 2.3, and can act as a PCI master and target. Furthermore, it implements PCI bus arbitration, supporting up to seven PCI bus agents, PCI reset signal generation, and all types of PCI transactions provisioned by the standard.

The PCI-HB builds on more than 15 years of CAST PCI IP expertise and has been designed for straightforward reuse, with proven design practices that ensure easy integration and smooth technology mapping. The core is available in synthesizable RTL or as a targeted FPGA netlist, and is delivered with everything required for rapid and successful integration and implementation.

Block Diagram

Implementation Results

PCI-HB reference designs have been evaluated in a variety of technologies. The following are sample Lattice results for the following configuration: single base address register configuration & support for 8 bus masters:

Lattice Device	LUT4s	Registers	Slices	SysMEM EBRs	External I/Os	Speed (f_{max}, MHz)
LFSC3GA25E-6	1569	649	1187	-	65	33
LFE2-50E-6	1357	590	1029	-	65	33
LFEC6E-4	1417	594	1061	-	65	33
LFXP6C-4	1417	594	1061	-	65	33
LCMXO280C-4	1177	590	790	-	65	33

See the web site for other implementation results.

Verification

The core has been verified through extensive simulation, rigorous code coverage measurements and it has been proven in FPGA and ASIC designs.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Lattice version includes:

- Post-synthesis netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration

CAST PCI Cores Family

CAST offers a broad family of PCI cores the members of which along with their basic features are outlined in the following table.

	PCI-T32	PCI-T32MF	PCI-M32	PCI-M32MF	PCI-HB	PCI-HB-AHB	PCI-DHB-AHB
PCI 33 MHz	✔	✔	✔	✔	✔	✔	✔
Host	✖	✖	✖	✖	✔	✔	✔
Master	✖	✖	✔	✔	✖	✖	✔
Target	✔	✔	✔	✔	✖	✖	✔
Multifunction	✖	✔	✖	✔	✖	✖	✖
32bit	✔	✔	✔	✔	✔	✔	✔
64bit	✖	✖	✖	✖	✖	✖	✖
SoC Interface	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AHB, AXI, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, Avalon-MM[1]	AHB	AHB
ASIC Support	✔	✔	✔	✔	✔	✔	✔
FPGA Support	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]

Notes:
- ✔ : Feature is supported
- ✔ : Feature optionally supported
- ✖ : Feature is not supported
- 1 : SoC interface in grey font can be made available upon request
- 2 : FPGA devices that do not support PCI I/O standard (e.g. Xilinx Virtex-6 and Stratix-V) are not supported