

CAST

PCI-HB-AHB

32-bit, 33/66MHz PCI - AMBA AHB Host Bridge Core

Features

- PCI specification 2.3 compliant
- 33/66 MHz performance
- 32-bit datapath
- PCI reset generator
- PCI bus arbiter (up to 7 external bus agents)
- Interrupt controller
- Parity generation and parity error detection.
- AMBA AHB host interface compliant with AMBA specification revision 2.0
- Unrelated AMBA and PCI clocks
- PCI Configuration registers accessible from both PCI and host directions
- Available in synthesizable VHDL source code

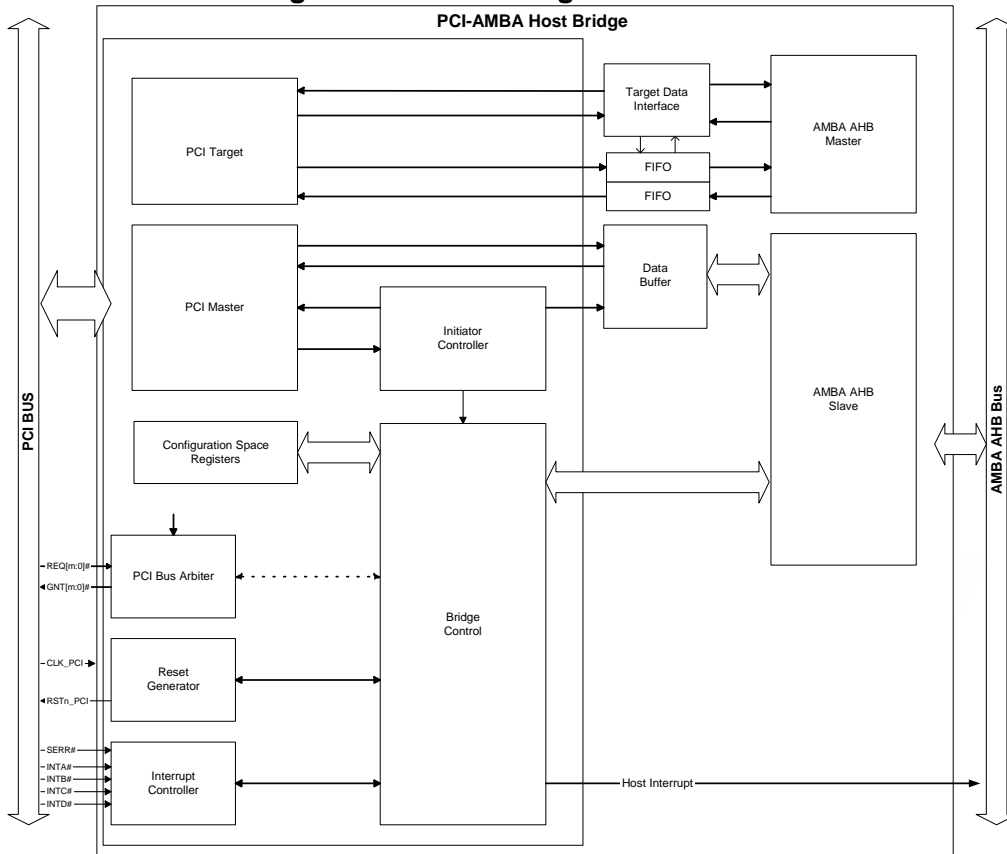
The PCI-HB-AHB core enables data transfers between a host processor system and PCI bus based devices. The bridge is in charge of PCI bus arbitration, generating PCI clock and reset signals. An important part of the bridge is the bus arbiter. The PCI-HB-AHB core enables data transfers between an AMBA AHB host processor bus system and PCI bus based devices. The bridge is in charge of PCI bus arbitration, generating PCI clock and reset signals. An important part of the bridge is the bus arbiter.

Applications

The PCI-HB-AHB can be utilized in a variety of PCI Interface applications including:

- Embedded system applications with PCI peripheral bus

PCI AMBA Host Bridge Architecture Diagram



Functional Description

The PCI AMBA host bridge architecture diagram describes a full bridge, which consists of generic PCI bridge core and user dependent parts (Target Data Interface, Dual-port memory and Host bus interface).

Configuration Space Registers

The Configuration Space Registers block implements the mandatory 64 bytes of the PCI Configuration Space registers. The registers can be accessible from both the PCI bus and the host bus.

PCI Master

The PCI master initiates PCI bus transactions. Transaction parameters are delivered from the Initiator controller (will be discussed later).

PCI Target

The PCI target data interface enables access to the host address space from the PCI bus agents (cards).

PCI Bus Arbiter

The PCI Bus arbiter grants a PCI bus mastership to one of the bus agents. The arbiter has to grant mastership to the PCI-HB core when the bus is idle to park the bus. There are optional features, which can be implemented in the bridge:

- Different schemes of bus granting (fixed priority, adjustable priority)
- Master agent malfunction detection and reporting (bus master agent requested mastership but does not initiate transaction when granted)

Reset Generator

The reset signal has to be asserted for a minimum of 1ms after power-up. The PCI specification defines that the PCI agents has to be ready to receive the first configuration transactions within 2^{25} PCI Clock cycles after reset.

Interrupt Controller

The interrupt controller monitors the PCI interrupt signals (INTx#) and the PCI system error signal (SERR#). Host interrupt assertion is controlled by an interrupt mask register.

Bridge Control

The bridge control block controls all the bridge functions and an interrupt propagation from the PCI side to the host processor system.

Initiator controller

The Initiator controller is the heart of the bridge. The controller has to be able to initiate the following transactions:

- Configuration space read/write
- Memory space read/write
- I/O Space read/write
- Interrupt acknowledge (optional)
- Special cycles (optional)

The controller has a set of registers, which define transaction parameters and a starting address of the data in a dual-port memory.

Target Data Interface

The target data interface controls a data buffering and clock domain crossing between the PCI Target and the AMBA interface.

AMBA AHB Master

The AHB master initiates transactions on the AHB bus, when requested by the target data interface.

AMBA AHB Slave

The AHB slave processes PCI bus access requests initiated by a host processor and access to the bridge control registers. PCI I/O space and memory space are mapped directly to the AMBA AHB memory space. An external AMBA address decoder has to be used for address space decoding and slave select signals control.

PCI bus arbitration

The PCI bus arbitration is controlled by a PCI bus arbiter. The arbiter supports up to eight masters. The bridge's PCI interface is internally connected to the arbiter. The arbiter uses the bridge's PCI interface core as a default PCI bus park master.

PCI bus reset

The PCI bus reset is a process where the host bridge has to assert *rstno*. There are certain timing constraints for the reset process. The reset signal *rstno* has to be asserted at least 1ms after power-up. The bridge is ready to initiate the first configuration access after 2^{25} clock cycles from the reset signal deassertion. The host bridge readiness to perform PCI transactions is indicated in the bridge status register.

PCI bus clock

The PCI-HB-AHB core does not contain a PCI bus clock generator since the implementation is application dependent. The PCI clock can be derived from a host clock or generated by an external clock source. The PCI bus clock has to follow PCI bus specification.

Implementation Results

PCI-HB-AHB reference designs have been evaluated in a variety of technologies. The following are representative ASIC results.

ASIC Technology	Cell Area	NAND2 Area	Approx. Area (gate equiv.)	Frequency (MHz) PCI Clock
TSMC 65 nm	31,778	1.6	19,861	66
TSMC .09 μ m	49,920	2.8224	17,700	66
TSMC .13 μ m	98,308	5.0922	19,300	66
TSMC .18 μ m	206,616	9.9792	20,700	66

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide