PCI-DHB-AHB
PCI - AMBA AHB Device/Host Bridge Core

This PCI Host Bridge IP core enables data transfers between an AMBA® AHB host processor bus system and PCI bus based devices.

The bridge supports Host Mode and Device Mode (selected by a dedicated input pin). In Host Mode, the bridge is in charge of PCI bus arbitration and generating the PCI reset signal. In Device Mode, the bridge implements a PCI target enabling PCI access to the AMBA AHB bus space behind the bridge.
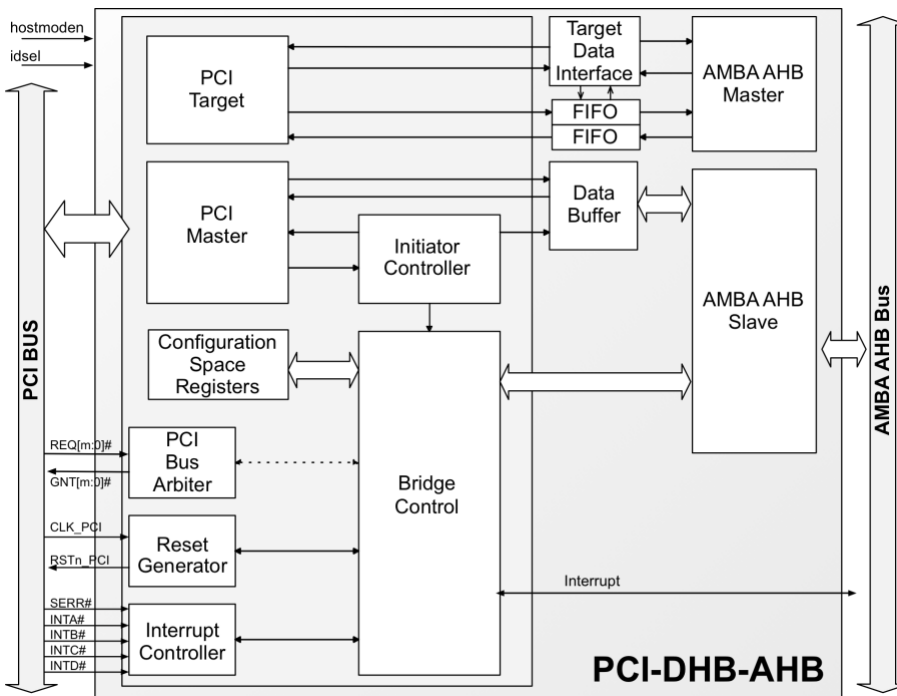
The bridge enables higher utilization of the bus' available bandwidth by prefetching PCI data and buffering AHB data, and allows the host to initiate PCI accesses or to respond to transactions initiated by other PCI devices.

The core complies with the PCI bus specification versions 3.0 and 2.3, and can act as a PCI master and target. Furthermore, it implements PCI bus arbitration, supporting up to seven PCI bus agents, PCI reset signal generation, and all types of PCI transactions provisioned by the standard.

The host connects to the bridge via master and a slave 32-bit AMBA/AHB bus interfaces. The AHB slave interface allows the host to access the status and to control registers and initiate PCI Transfers, while data from the PCI target is communicated to the host via the AHB master interface.

The PCI-DHB-AHB builds on more than 15 years of CAST PCI IP expertise and has been designed for straightforward reuse, with proven design practices that ensure easy integration and smooth technology mapping. The core is available in synthesizable RTL or as a targeted FPGA netlist, and is delivered with everything required for rapid and successful integration and implementation.

Block Diagram

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Implementation Results

PCI-DHB-AHB reference designs have been evaluated in a variety of technologies. The following are indicative ASIC results.

ASIC Technology	Cell Area (um^2)	Approx. Area (gate equiv.)	Frequency (MHz) PCI Clock
TSMC 65 nm	45468	28,417	66
TSMC .09 µm	73586	26,072	66
TSMC .13 µm	149607	29.379	66

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation, rigorous code coverage measurements and it has been proven in FPGA and ASIC designs.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

CAST PCI Cores Family

CAST offers a broad family of PCI cores the members of which along with their basic features are outlined in the following table

	PCI-T32	PCI-T32MF	PCI-M32	PCI-M32MF	PCI-HB	PCI-HB-AHB	PCI-DHB-AHB
PCI 33 MHz	✔	✔	✔	✔	✔	✔	✔
Host	✕	✕	✕	✕	✔	✔	✔
Master	✕	✕	✔	✔	✕	✕	✔ (optional)
Target	✔	✔	✔	✔	✕	✕	✔ (optional)
Multifunction	✕	✔	✕	✔	✕	✕	✕
32bit	✔	✔	✔	✔	✔	✔	✔
64bit	✕	✕	✕	✕	✕	✕	✕
SoC Interface	Generic AXI, AHB, Avalon-MM1	Generic AXI, AHB, Avalon-MM1	Generic AHB, AXI, Avalon-MM1	Generic AXI, AHB, Avalon-MM1	Generic AXI, Avalon-MM1	AHB	AHB
ASIC Support	✔	✔	✔	✔	✔	✔	✔
FPGA Support	✔2	✔2	✔2	✔2	✔2	✔2	✔2

Notes:
- ✔ : Feature is supported
- ✔ (grey) : Feature optionally supported
- ✕ : Feature is not supported
- 1 : SoC interface in grey font can be made available upon request
- 2 : FPGA devices that do not support PCI I/O standard (e.g. Xilinx Virtex-6 and Stratix-V) are not supported