

CAST

MTS-E

MPEG Transport Stream Multiplexing & Encapsulation Engine

Features

MPEG Transport Stream Multiplexing & Encapsulation

- Compliant to ISO/IEC 13818-1
- Two input stream channels (additional channels upon request)
- Supports common stream types
 - Audio
 - Video
 - Metadata
- Flexible Encapsulation
 - Programmable Packetized Elementary Stream (PES) packet size
 - Programmable TS packet group size
 - Optional Program Info support
 - Optional Elementary Stream Info support

RTP Encapsulation

- Software enabled/disabled encapsulation of the MPEG Transport stream in RTP packets

Easy Integration

- Standalone, processor-less operation
- AMBA® AXI Interfaces
- AXI4-Lite™ Control/Status register interfaces
- AXI4-Streaming™ interfaces for packet data
- Optional Avalon® SoC bus interface
- Configurable input and output buffers sizes
- The MTS-E can be delivered pre-integrated with:
 - Video Encoder cores from CAST
 - UDP/IP Hardware Stack from CAST, and eMAC core from Altera, Xilinx, or other third-party

The MTS-E core multiplexes and encapsulates audio, video and metadata streams in a single MPEG Transport Stream (TS), and optionally encapsulates the TS packets in Real-Time Transport Protocol (RTP) packets.

Under its default configuration, the MTS-E multiplexing and encapsulation engine supports two input stream channels, e.g., one Audio and one Video. Configurations with more than two input stream channels can be made available upon request.

The output transport stream can be forwarded for local storage or transmitted over an Internet Protocol (IP) or other network. Streaming over IP networks often imposes further encapsulation of the transport stream in RTP, UDP, and IP packets. The MTS-E core can be programmed to perform RTP encapsulation, while the companion UDP/IP core from CAST supports UDP/IP encapsulation.

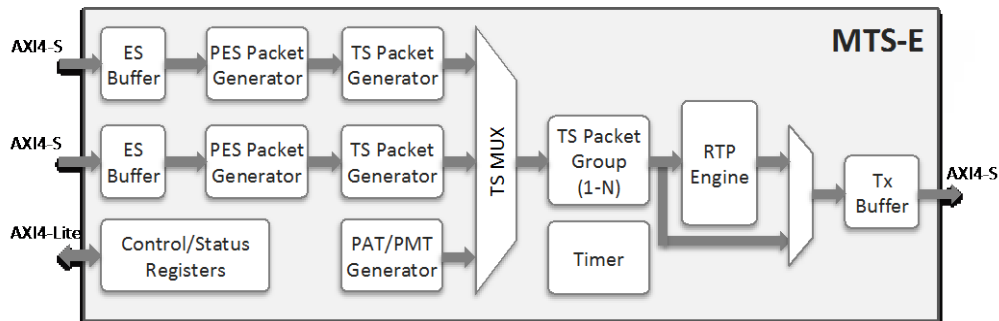
The core is easy to integrate in systems with or without a host processor. Once configured via its control registers, the MTS-E operates on a standalone basis. Input streams and TS/RTP packet output are sent via dedicated AXI4-Streaming interfaces, enabling direct connection to hardware media encoders and hardware stacks for UDP or TCP. Status and control registers are accessible by an AXI4-Lite interface.

The MTS-E core is available in RTL source or as a targeted FPGA netlist. Subsystems integrating the core with H.264 encoder, UDP/IP, and eMAC cores are also available from CAST, and can enable rapid video over IP systems development.

Applications

The versatile MTS-E core is especially suitable for video conferencing systems, surveillance systems, and other multi-channel media streaming applications and devices featuring media streaming over IP networks.

Block Diagram



Functional Description

The MTS-E core multiplexes and encapsulates input audio, video, or metadata streams to a single TS stream, and optionally encapsulates the TS stream into RTP packets. The core consists of the following modules.

PES Packet Generator – Generates Programmable Packetized Elementary Stream (PES) packets from the incoming Audio or Video stream. It performs data buffering, PES packet sizing, and splitting, and also adds timing information to the PES packet header for each new video frame or audio packet.

TS Packet Generator – Fragments PES packets to the Transport Stream (TS) packet payload and adds the correct TS header to each TS packet. It is also responsible for adding Program Clock Reference (PCR) and padding TS packets, which are not fully filled with the stream data payload.

PAT/PMT Packet Generator – Assembles and periodically generates Program Association Table (PAT) TS packets and Program Map Table (PMT) TS packets based on the control register parameters.

TS Packet Multiplexer – Provides multiplexing between Stream 0, Stream 1, and PAT/PMT TS packets.

TS Packet Group module – Performs TS packet grouping for UDP or RTP transmission. The grouped TS packets are either sent outside the MTS-E core or further encapsulated into the RTP packets.

RTP Module – Performs encapsulation of the grouped TS packets into RTP packets.

System Timer – Generates timestamps for audio and video streams as well as the RTP timestamp when RTP is enabled. The timer allows delay adjustment between the audio and video streams to compensate for different audio and video encoding latency. The timer is also responsible for PAT/PMT and PCR timing.

Output Multiplexer – Selects between the TS packet and RTP packet output format.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

MTS-E reference designs have been evaluated in a variety of technologies. The following are sample ASIC pre-layout results reported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip. These sample results do not represent the highest speed or smallest area for the core.

ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Memory Bits
TSMC 65nmG	8,322	612	65,536
TSMC 90nmG	7,714	360	65,536

Table 1: MTS-E configured with one input stream channel, no RTP, no TS packet grouping and no Program and ES info support.

ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Memory Bits
TSMC 65nmG	19,096	616	150,016
TSMC 90nmG	17,792	360	150,016

Table 2: MTS-E configured with two input stream channel, RTP, TS packet grouping and no Program and ES info support.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.

Related Cores

- H.264 Video Encoder Cores:
[Baseline](#), [Main](#), and [High](#) Profiles
- [UDPIP](#): UDP/IP Hardware Protocol Stack Core

Contact CAST Sales to discuss how our IP integration services can save you even more time with any of these multi-core combinations.