

CAST

MAC

Ethernet Media Access Controller Core

Implements a high-speed (10/100 Mbps), half- and full-duplex LAN controller using the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by IEEE 802.3 for media access control over the Ethernet.

For broad compatibility and easy integration, the core works with any MII-compliant external PHY transceiver. (SMII & RMII support is available.)

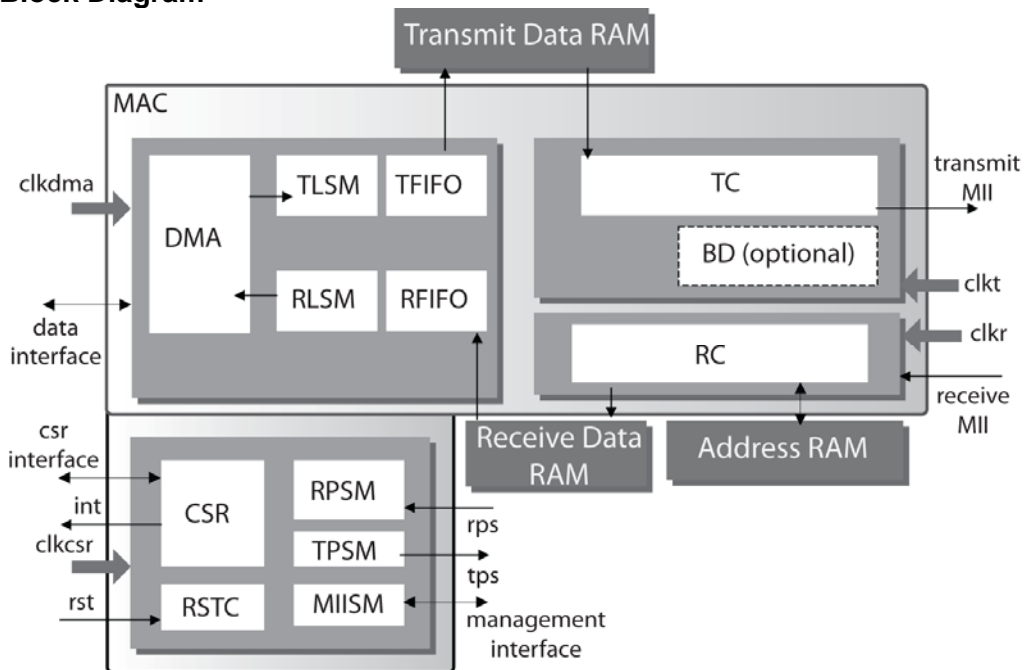
The core has a generic host-side interface designed for easy compatibility with a variety of external CPUs or standard bus controllers such as PCI. This host interface can be configured to work with 8-, 16- or 32-bit data bus lengths with big or little endian byte ordering, and is compatible with most modern virtual component interfaces. Optional standard interfaces such as AMBA, OCP, and OPB are available.

The MAC was developed for reuse in ASIC and FPGA implementations and has been implemented in several commercial products. The design is strictly synchronous with positive-edge clocking, no internal tri-states and with a synchronous reset.

Applications

The MAC core can be utilized for a variety of interface applications including network Interface Cards (NICs); routers and switching hubs; and many Systems On Chip (SoC) applications.

Block Diagram



Features

- Network interface features
 - Supports 10/100Mb/s data transfer rates
 - Media Independent Interface (MII)
 - Optional Reduced Media Independent Interface (RMII)
- Data link layer functionality
 - Meets the IEEE 802.3 CSMA/CD standard
 - Full or half duplex operation
 - Flexible address filtering
 - External RAM for storing MAC addresses
 - Up to 16 physical addresses
 - 512 bit hash table for multi-cast addresses
- Control and status registers
 - Configurable 8/16/32 bit slave interface
 - Single interrupt line
 - Interrupt mitigation control mechanism
- DMA controller
 - Configurable 8/16/32 bit data bus length
 - Configurable address bus length
 - Big or little endian data byte ordering
 - Scatter/gather capabilities
 - Programmable burst length
 - Intelligent arbitration between transmit and receive processes
- Descriptor/buffer architecture for data storage
 - Descriptor "ring" or "chain" structures
 - Automatic descriptor list pooling
- Transmit/Receive dual port RAM interfaces
 - Operates as internal configurable FIFOs
 - Programmable threshold levels
 - "Store and forward" functionality
- Optional standard bus interfaces include AMBA, OCP, and OPB
- Optional Linux driver

Functional Description

The MAC core consists of the following components as shown in the block diagram:

TC - Transmit Controller

Implements the 802.3 transmit operation and uses the standard 802.3 MII interface for an external PHY device. Operates synchronously with the clk clock from the MII interface.

BD - Backoff/Deferring

Implements the 802.3 half-duplex operation. Operates synchronously with the clk clock from the MII interface. Can be removed for lower gate count if the half-duplex operation is not required.

RC - Receive Controller

Implements the 802.3 receive operation using the standard 802.3 MII interface for an external PHY device. Operates synchronously with the clkr clock from the MII interface.

TFIFO - Transmit FIFO

Buffers data prepared for transmission by the MAC. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: TFIFODEPTH defines the total FIFO size; TCDEPTH defines the maximum number of frames that can reside in the transmit FIFO at the moment. Operates synchronously with the clkdma clock from the host Data interface.

RFIFO - Receive FIFO

Buffers data received by the MAC. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: RFIFODEPTH defines the total FIFO size; RCDEPTH defines the maximum number of frames that can reside in the receive FIFO at the moment. Operates synchronously with the clkdma clock from the host Data interface.

TLSM - Transmit linked List State Machine

Implements the descriptor/buffer architecture of the MAC. It manages the transmit descriptor list, and fetches the data prepared for transmission from the data buffers into the transmit FIFO. Operates synchronously with the clkdma clock from the host Data interface.

RLSM - Receive linked List State Machine

Implements the descriptor/buffer architecture of the MAC. It manages the receive descriptor list, and moves the data the receive FIFO into the data buffers. Operates synchronously with the clkdma clock from the host Data interface.

DMA - Direct Memory Access Controller

Implements the host Data interface, servicing both the receive and the transmit channels. Operates synchronously with the clkdma clock from the host Data interface.

CSR - Control and Status Registers

Used by the host to control the MAC operation. Implements the register set, the interrupt controller, and the power management functionality of the MAC, and provides an interface for the host. Operates synchronously with the clkcsr clock from the host CSR interface.

RSTC - Reset Controller

Resets all components of the MAC. It generates reset signal synchronous to all clock domains in the design from the single external reset line.

MIISM – MII Serial Management

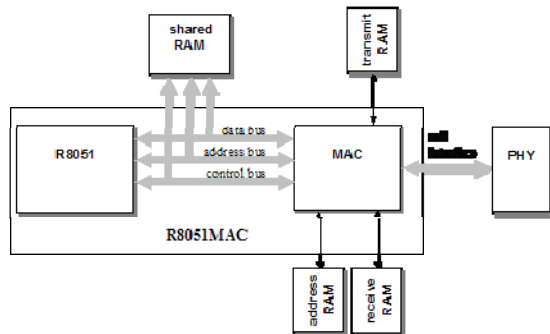
The MIISM interface controller is a module for the MAC that provides a simple serial communication interface between the MAC and the PHY(s). The module supplies the hardware controlled protocol to read and/or write the status and configuration registers in the PHY layer implementation.

External Components

There are three external components required for proper operation of the MAC core:

- Receive data RAM: synchronous dual port RAM working as receive FIFO.
- Transmit data RAM: synchronous dual port RAM working as transmit FIFO.
- Address RAM: synchronous dual port RAM working as MAC addresses memory.

Pre-Integrated IP Platform – R8051MAC



The R8051MAC Controller combines the MAC with an 8051-compatible core and is useful for quickly implementing Ethernet devices in many applications. The 8051 operates as a system host, communicating with the MAC through shared RAM memory and by direct interface to its Control and Status Registers (CSRs). The complete platform consists of the R8051MAC core together with the following components:

- Dual port RAMs for transmit FIFO, receive FIFO and address filtering RAM.
- External PHY transceiver for connection with Ethernet network.
- Shared RAM, which stores data buffers and descriptor list.

Configurability

The following parameters allow adjusting the MAC to the requirements of the target application or technology:

- CSR data bus width – 8 or 16 or 32
- data interface bus width – 8 or 16 or 32
- data interface address bus width – 8 to 32
- transmit FIFO size – 64B to 64kB
- receive FIFO size – 64B to 64kB

Options

Following optional modules may be ordered according to the user's application:

- RMI - Reduced MII interface instead of standard MII
- SMII - Serial MII interface instead of standard MII
- FC – Flow Control
- SC - Statistical Counters Controller
- FCSTAT – Flow Control Statistics

Core Modifications

The FIFO memories can be resized according to Ethernet network requirements. External host interfaces can be customized for use in 8-, 16- or 32-bit systems. Contact CAST for any required modifications.

Implementation Results

The core has been successfully implemented in a variety of products and reference designs. Results for a typical configuration (with no memories) optimized for speed are shown here.

ASIC Technology	Optimization Strategy	Approx. Area	Frequency (APB clock)
TSMC 0.18 μ m	Area	39,000 gates	50 MHz
TSMC 0.18 μ m	Speed	46,000 gates	147 MHz

See the web site for FPGA and other implementation results.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench, including the core and:
 - On-chip dual-port RAMs
 - Bus/behavioral models of the host, shared RAM, and PHY devices
 - Clock generator
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide