

CAST



MAC

10/100 Ethernet Media Access Controller Core

Implements a high-speed (10/100 Mbps), half- and full-duplex LAN controller using the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by IEEE 802.3 for media access control over the Ethernet.

For broad compatibility and easy integration, the core works with any MII-compliant external PHY transceiver. (SMII & RMII support is available.)

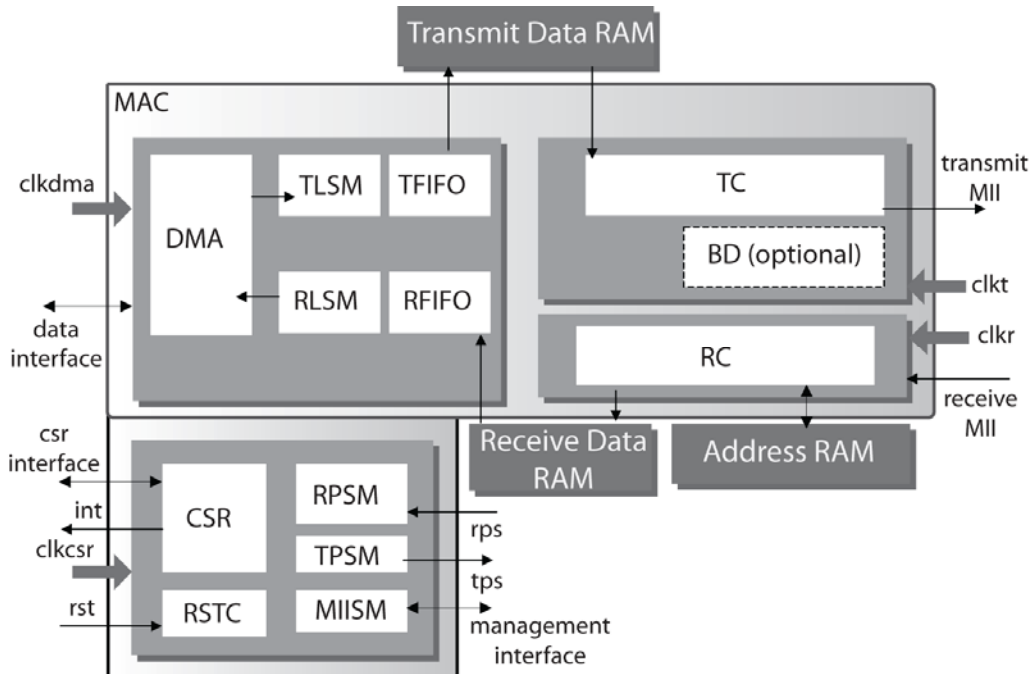
The core has a generic host-side interface designed for easy compatibility with a variety of external CPUs or standard bus controllers such as PCI. This host interface can be configured to work with 8-, 16- or 32-bit data bus lengths with big or little endian byte ordering, and is compatible with most modern virtual component interfaces. Optional standard interfaces such as AMBA, OCP, and OPB are available.

The MAC was developed for reuse in ASIC and FPGA implementations and has been implemented in several commercial products. The design is strictly synchronous with positive-edge clocking, no internal tri-states and with a synchronous reset.

Applications

The MAC core can be utilized for a variety of interface applications including network Interface Cards (NICs); routers and switching hubs; and many Systems On Chip (SoC) applications.

Block Diagram



Features

- Network interface features
 - ▶ Supports 10/100Mb/s data transfer rates
 - ▶ Media Independent Interface (MII)
 - ▶ Optional Reduced Media Independent Interface (RMII)
- Data link layer functionality
 - ▶ Meets the IEEE 802.3 CSMA/CD standard
 - ▶ Full or half duplex operation
 - ▶ Flexible address filtering
 - ▶ External RAM for storing MAC addresses
 - ▶ Up to 16 physical addresses
 - ▶ 512 bit hash table for multi-cast addresses
- Control and status registers
 - ▶ Configurable 8/16/32 bit slave interface
 - ▶ Single interrupt line
 - ▶ Interrupt mitigation control mechanism
- DMA controller
 - ▶ Configurable 8/16/32 bit data bus length
 - ▶ Configurable address bus length
 - ▶ Big or little endian data byte ordering
 - ▶ Scatter/gather capabilities
 - ▶ Programmable burst length
 - ▶ Intelligent arbitration between transmit and receive processes
- Descriptor/buffer architecture for data storage
 - ▶ Descriptor "ring" or "chain" structures
 - ▶ Automatic descriptor list pooling
- Transmit/Receive dual port RAM interfaces
 - ▶ Operates as internal configurable FIFOs
 - ▶ Programmable threshold levels
 - ▶ "Store and forward" functionality
- Optional standard bus interfaces include AMBA, OCP, and OPB
- Optional Linux driver

Functional Description

The MAC core consists of the following components as shown in the block diagram:

TC - Transmit Controller

Implements the 802.3 transmit operation and uses the standard 802.3 MII interface for an external PHY device. Operates synchronously with the clkt clock from the MII interface.

BD - Backoff/Deferring

Implements the 802.3 half-duplex operation. Operates synchronously with the clkt clock from the MII interface. Can be removed for lower gate count if the half-duplex operation is not required.

RC - Receive Controller

Implements the 802.3 receive operation using the standard 802.3 MII interface for an external PHY device. Operates synchronously with the clkr clock from the MII interface.

TFIFO - Transmit FIFO

Buffers data prepared for transmission by the MAC. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: TFIFODEPTH defines the total FIFO size; TCDEPTH defines the maximum number of frames that can reside in the transmit FIFO at the moment. Operates synchronously with the clkdma clock from the host Data interface.

RFIFO - Receive FIFO

Buffers data received by the MAC. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: RFIFODEPTH defines the total FIFO size; RCDEPTH defines the maximum number of frames that can reside in the receive FIFO at the moment. Operates synchronously with the clkdma clock from the host Data interface.

TLSM - Transmit linked List State Machine

Implements the descriptor/buffer architecture of the MAC. It manages the transmit descriptor list, and fetches the data prepared for transmission from the data buffers into the transmit FIFO. Operates synchronously with the clkdma clock from the host Data interface.

RLSM - Receive linked List State Machine

Implements the descriptor/buffer architecture of the MAC. It manages the receive descriptor list, and moves the data the receive FIFO into the data buffers. Operates synchronously with the clkdma clock from the host Data interface.

DMA - Direct Memory Access Controller

Implements the host Data interface, servicing both the receive and the transmit channels. Operates synchronously with the clkdma clock from the host Data interface.

CSR - Control and Status Registers

Used by the host to control the MAC operation. Implements the register set, the interrupt controller, and the power management functionality of the MAC, and provides an interface for the host. Operates synchronously with the clkcsr clock from the host CSR interface.

RSTC - Reset Controller

Resets all components of the MAC. It generates reset signal synchronous to all clock domains in the design from the single external reset line.

MIISM – MII Serial Management

The MIISM interface controller is a module for the MAC that provides a simple serial communication interface between the MAC and the PHY(s). The module supplies the hardware controlled protocol to read and/or write the status and configuration registers in the PHY layer implementation.

External Components

There are three external components required for proper operation of the MAC core:

- Receive data RAM: synchronous dual port RAM working as receive FIFO.
- Transmit data RAM: synchronous dual port RAM working as transmit FIFO.
- Address RAM: synchronous dual port RAM working as MAC addresses memory.

Configurability

The following parameters allow adjusting the MAC to the requirements of the target application or technology:

- CSR data bus width – 8 or 16 or 32
- data interface bus width – 8 or 16 or 32
- data interface address bus width – 8 to 32
- transmit FIFO size – 64B to 64kB
- receive FIFO size – 64B to 64kB

Options

Following optional modules may be ordered according to the user's application:

- RMII - Reduced MII interface instead of standard MII
- SMII - Serial MII interface instead of standard MII
- FC – Flow Control
- SC - Statistical Counters Controller
- FCSTAT – Flow Control Statistics

Implementation Results

The following are typical performance and utilization results for Lattice ispXPGA™ devices. (This typical 32-bit configuration includes 2x2Kb of FIFO memory and 512 bytes of address filtering RAM.)

Lattice Device	LUT4s	Registers	PFUs	Slices	SysMEM EBRs	External I/Os	Speed (fmax, MHz)
LFX1200C-3	7715	2271	2085	-	9	258	36.15
LFXP15C-5	3384	2161	-	3777	2	258	69

See the web site for other implementation results.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF netlist (firm core) optimized for a specific Lattice device (HDL RTL source code (soft core) is also available)
- Sophisticated HDL Testbench, including the core and:
 - On-chip dual-port RAMs
 - Bus/behavioral models of the host, shared RAM, and PHY devices
 - Clock generator
- Simulation script, vectors, and expected results
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 076747 USA
tel 201-391-8300 fax 201-391-8694
Copyright © CAST, Inc. 2009, All Rights Reserved.
Contents subject to change without notice. November 2003



<http://www.latticesemi.com>