

CAST



MAC-PCI

Ethernet MAC Controller with PCI Host Interface Core

The MAC-PCI IP core is a combination of the Ethernet Media Access Controller (MAC) HDL core - and the 32-bit 33 MHz Master/Slave PCI Host Interface core (PCI-M32). The core is intended to simplify the Ethernet networking support development in PCI based systems and applications.

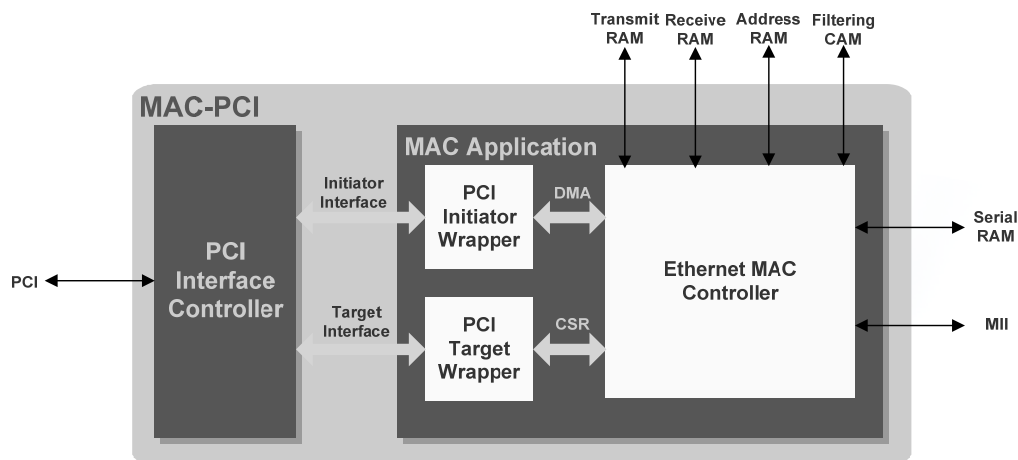
A variety of available PHY interfaces facilitates the controller's integration with a wide range of third-party transceivers. While the implementation of the most common PCI Local Bus interface guarantees seamless integration with a large number of PCI-equipped hardware devices, an available Linux driver allows users to skip basic software development stages and concentrate on designing the main application. Both the integrated scatter/gather DMA Controller and extended filtering features decrease CPU overhead, whereas advanced interrupt mitigation lowers the number of necessary interrupt support routines. Configurable internal FIFO's architecture and low power capabilities make MAC-PCI a perfect solution for both resource and power limited applications.

The MAC-PCI is a design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states, and a synchronous reset; therefore, scan insertion is straightforward.

Applications

- PCI-based systems
- Network Interface Controllers

Block Diagram



Features

- Network Interface Features
 - Support for 10/100 Mbps data transfer rate
 - Media Independent Interface (MII) for 10/100 Mbps operation
 - Automated MII Management interface
- Data Link Layer Functionality
 - Support for the IEEE 802.3 CSMA/CD standard
 - Full or half duplex operation
 - Flexible address filtering
 - External RAM for storing MAC addresses
 - Up to 16 physical addresses
 - 512 bit hash table for multi-cast addresses
- PCI Local Bus Interface Support
 - PCI spec 2.3 compliant
 - 33 MHz performance
 - 32-bit data path
 - Zero wait states burst mode
 - Full bus master/target functionality
 - Single interrupt
 - Type 0 Configuration Space
 - Support for backend initiated target retry, disconnect and abort
- DMA Controller
 - Scatter/gather capabilities
 - Programmable burst length
 - Intelligent arbitration between transmit and receive processes
- Descriptor / Buffer Architecture for Data Storage
 - Descriptor "ring" or "chain" structures
 - Single descriptor can point to two data buffers
 - Auto descriptor list pooling
- Low Power Capabilities
 - Independent clocks for data and control paths
 - Running/Suspended/Stopped modes of operation
 - Clock switching support
- Transmit/Receive Dual Port RAM Interfaces
 - Operating as internal configurable FIFO's
 - Programmable threshold levels
 - "Store and forward" functionality
- Dedicated Linux Driver

January 2009

Functional Description

The core consists of functional blocks as shown in the diagram and briefly described here.

Ethernet MAC Controller

The MAC subcomponent consists of several modules that provide MAC-PCI with essential Ethernet functionality. Transmit/Receive Controllers implement frames operations according to IEEE 802.3 CSMA/CD standard, while an optional Backoff/Deferring component implements half-duplex functions. Transmit/Receive FIFO's handle data buffering and provide an interface for external dual-port RAM, working as FIFO memory. Transmit/Receive List State Machines implement descriptors/buffers for architecture handling over a built-in DMA Controller, which provides the Ethernet MAC with master data interface to service both receive and transmit channels. Control and Status Registers implement the register set, interrupt controller, serial RAM and MII management interfacing, and power management functionality.

PCI Interface Controller

The PCI subcomponent handles the PCI Local bus transaction. It consists of several modules that implement particular functions: initiating and handling PCI transactions, parity bits generation and checking, and PCI configuration space handling.

PCI Initiator Wrapper

The module provides the FSM and logic required to translate DMA master interface transfers into PCI bus transactions.

PCI Target Wrapper

The module provides FSM and logic essential for translating PCI transactions into the generic MAC CSR slave interface transfers.

Configurability

The following parameters allow adjusting the MAC-PCI core to requirements of target application or technology:

- transmit FIFO size – 128B to 64kB
- receive FIFO size – 128B to 64kB

Options

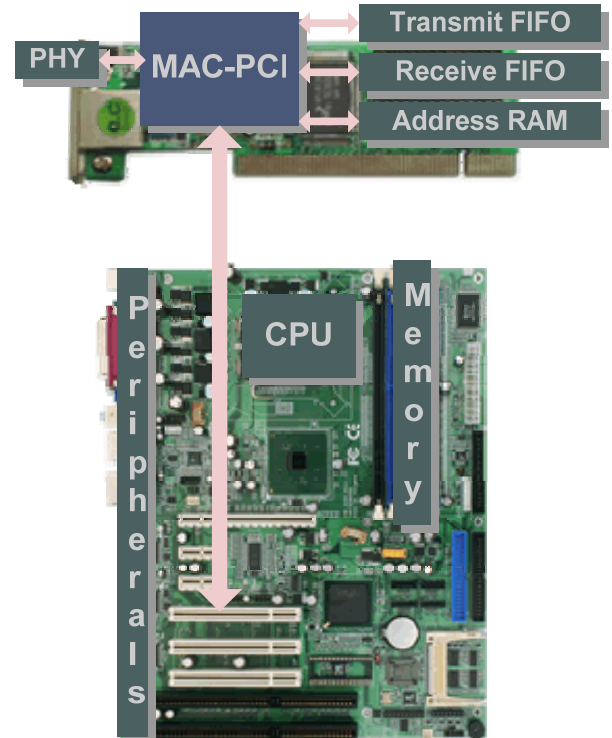
- RMII - Reduced MII interface, instead of standard MII
- SMII - Serial MII interface, instead of standard MII
- Slightly modified version of the original Linux kernel integrated Tulip driver that adds a special MAC address reading routine
- An evaluation system including board and software
- Reference design for a proprietary development board

Example Application

The MAC-PCI controller is used to implement 10 and 100 Mbps Ethernet networks interface in a PCI-enabled system. The example application consists of the microprocessor, shared memory block, and the MAC-PCI core.

The host application communicates with the MAC-PCI through a set of Control and Status Registers (CSRs), connected to the PCI Bus shared with other system peripherals.

To provide high system performance, the MAC's DMA engine is connected as a second PCI initiator device on the bus and automatically transfers the frames to and from buffers defined in a shared memory block.



Implementation Results

MAC-PCI reference designs have been evaluated in a variety of technologies. The following are sample Xilinx implementation numbers.

Xilinx Device	Slices	BRAM	I/Os	Fmax (MHz)	ISE
Spartan-3E XC3S1600E-4	2710	3	130	33	10.1i
Virtex-II Pro XC2VP40-7	2538	3	130	33	10.1i
Virtex-4 XC4VLX15-12	2544	3	130	33	10.1i
Virtex-5 XC5VLX30-3	1243	3	130	33	10.1i

Verification

The core has been verified through extensive functional and post-route simulation, and has achieved high Code Coverage. An FPGA prototype was used to verify the functionality in a Linux OS-based environment.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Place and route and simulation scripts
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verilog versions use Verilog 2001)
- Comprehensive documentation