

CAST



MAC-L

10/100 Ethernet Media Access Controller Lite Core

Features

The MAC-L Ethernet controller is a core of a high-speed LAN controller. It implements Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by IEEE 802.3 for media access control over the Ethernet.

For broad compatibility and easy integration, the core works with any MII-compliant external PHY transceiver (SMII & RMII support is available.)

The core has an interface for external dual port RAMs serving as configurable FIFO memories with separate memories for transmit and receive processes. Using the FIFOs additionally isolates the MAC from the external host and provides resolution in case of latency of the external bus.

From the host side the MAC-L uses a generic interface with independent transmit and receive paths. The flexible design allows for using the MAC-L in various applications, especially switching and low gate-count applications.

The MAC-L was developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and with a synchronous reset.

- Network interface features
 - ▶ Supports 10/100Mb/s data transfer rates
 - ▶ Media Independent Interface (MII)
 - Optional Reduced Media Independent Interface (RMII)
 - ▶ Optional Serial MII interface instead of standard (SMII)
- Data link layer functionality
 - ▶ Meets the IEEE 802.3 CSMA/CD standard
 - ▶ Full or half duplex operation
 - ▶ Flexible address filtering
 - ▶ External RAM for storing MAC-L addresses
 - ▶ Up to 16 physical addresses
 - ▶ 512 bit hash table for multi-cast addresses
 - ▶ External CAM interface
- Transmit/Receive dual port RAM interfaces
 - ▶ Operates as internal configurable FIFOs
 - ▶ Programmable threshold levels
 - ▶ "Store and forward" functionality

Applications

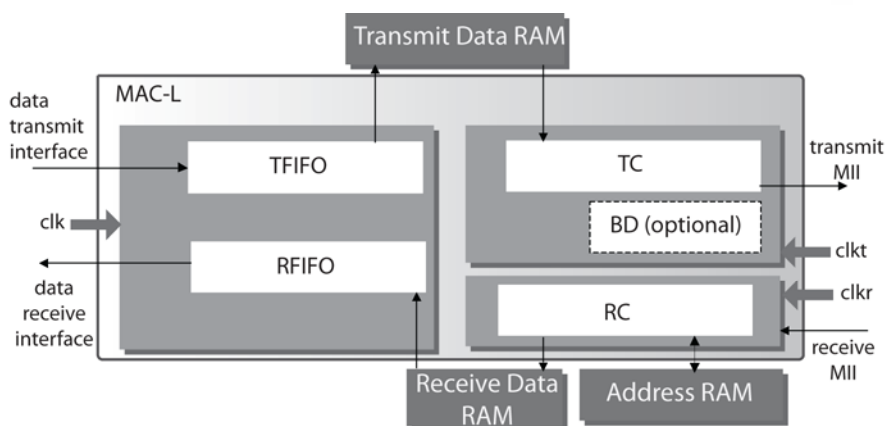
The MAC-L core can be utilized for a variety of applications including:

- Routers and Switching hubs
- Real-Time Industrial Ethernet Systems
- Low power digital acquisition systems sensors
- Avionics Full-Duplex Ethernet Communication (AFDX)

Benefits

- Very low gate count per instance makes the IP core an excellent choice for multiport Ethernet devices
- High configurability level makes the controller suitable for a large scope of SoC applications
- Variety of available physical layer interfaces - MII, SMII, RMII gives excellent support for different market solutions

Block Diagram



Functional Description

The MAC-L core is partitioned into modules as shown in the block diagram and described below.

TC – Transmit Controller

The transmit controller implements the 802.3 transmit operation. From the network side it uses the standard 802.3 MII interface for an external PHY device. The transmit controller operates synchronously with the *clkt* clock from the MII interface.

BD – Backoff/Deferring

The backoff/deferring controller implements the 802.3 half duplex operation. It operates synchronously with the *clkt* clock from the MII interface. The backoff/deferring controller can be optionally removed for lower gate-count if the half duplex operation is not required.

RC – Receive Controller

The receive controller implements the 802.3 receive operation. From the network side it uses the standard 802.3 MII interface for an external PHY device. The receive controller operates synchronously with the *clkr* clock from the MII interface.

TFIFO – Transmit FIFO

The transmit FIFO is used for buffering data prepared for transmission by the MAC-L. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core. The TFIFODEPTH parameter defines the total FIFO size. The TCDEPTH parameter defines the maximum number of frames that can reside in the transmit FIFO at the same time. The transmit FIFO controller operates synchronously with the *clk* host side clock.

RFIFO – Receive FIFO

The receive FIFO is used for buffering data received by the MAC-L. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core. The RFIFODEPTH parameter defines the total FIFO size. The RCDEPTH parameter defines the maximum number of frames that can reside in the receive FIFO at the same time. The receive FIFO controller operates synchronously with the *clk* host side clock.

External components

For proper operation of the core the following external components are required:

- Transmit Data RAM – Synchronous dual port RAM working as transmit FIFO memory
- Receive Data RAM – Synchronous dual port RAM working as receive FIFO memory
- Address RAM – Synchronous dual port RAM for MAC-L address memory

For more details concerning dual port RAMs refer to the “External dual-port RAM interface” section of the MAC-L User’s Guide.

Implementation Results

The following are typical performance and utilization results using Lattice ispXPGA™ and ORCA™ devices. (This typical 32-bit configuration includes 2x2Kb of FIFO memory and 512 bytes of address filtering RAM.)

| Lattice Device | LUT-4s | Registers | PFUs | SysMEM EBRs | External I/Os | Speed (f _{max} , MHz) |
|----------------|--------|-----------|------|-------------|---------------|--------------------------------|
| LFX500C-4 | 2596 | 979 | 2596 | 9 | 282 | 58.65 |

Options

The following optional modules may be ordered according to the user’s application:

- RMII - Reduced MII interface instead of standard MII
- SMII - Serial MII interface instead of standard MII

Configurability

The following parameters allow adjusting the MAC-L to the requirements of the target application or technology:

- data interface bus width – 8 or 16 or 32
- transmit FIFO size – 64B to 64kB
- receive FIFO size – 64B to 64kB

The core is delivered with a standard configuration including BD backoff/deferring module. The backoff/deferring controller can be easily removed for lower gate count if half duplex operation is not required.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core functionality was verified in a FPGA prototype working in an Ethernet 10/100 Mbit network.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF netlist (firm core) optimized for a specific Lattice device (HDL RTL source code (soft core) is also available)
- Testbenches (self-checking) that includes:
 - The MAC-L core with memories
 - Bus/behavioral models of host and PHY devices
 - Clock and reset generators
- Simulation script, vectors, and expected results
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation