

CAST



MAC-1G

1-Gigabit Ethernet Media Access Controller Core

The MAC-1G is a flexible, full-featured implementation of IEEE 802.3-2000 that operates at 10/100/1000 Mbps. It includes a generic host interface with integrated FIFO logic and DMA controller and can work with various data path widths and system clock speeds. It provides half- or full-duplex operation, supports jumbo frames, and includes low-power features. Its network interface supports any MII/GMII physical layer devices.

The core's optional AMBA interface is included in this Synplicity ReadyIP evaluation configuration.

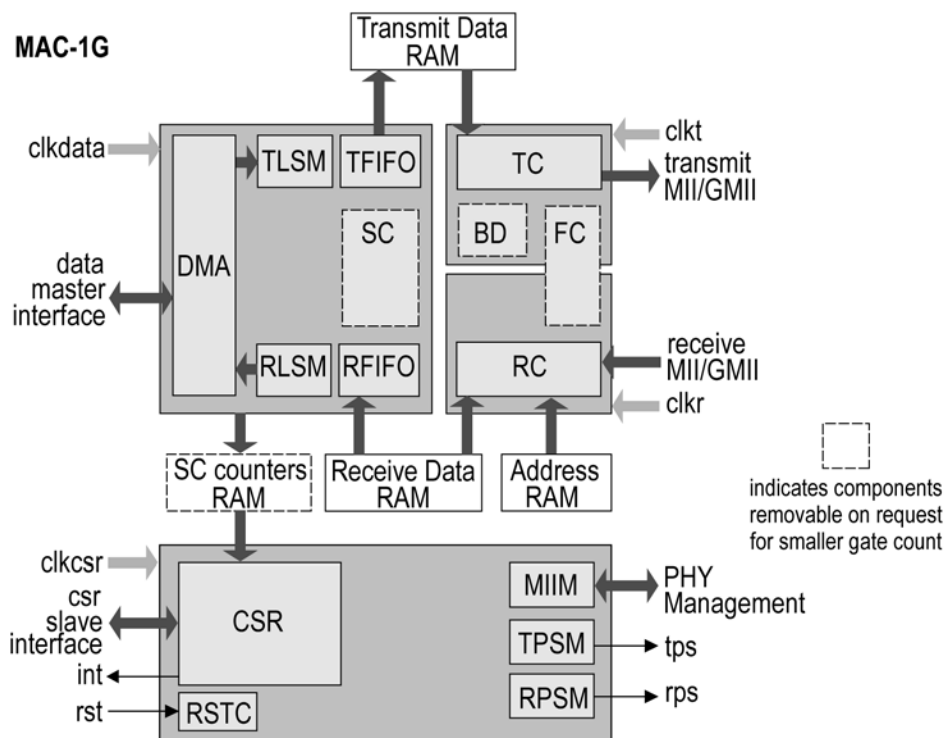
Designed for easy reuse, the core uses under 39,000 ASIC gates.

Applications

The MAC-1G is ready to serve as a complete network controller that designers can simply connect to any 8-, 16-, 32-, or 64-bit processor working with any arbitrary clock frequency. Specific applications include:

- Network Interface Cards (NICs)
- Routers, switching hubs
- Systems On Chip (SOCs)

Block Diagram



Features

- Network interface features
 - Supports data transfer rates of 10/100/1000 Mbps
 - GMII/RGMII Media Independent Interface
 - Optional RMII, SMII
 - PHY management interface*
- Data link layer functionality
 - Meets IEEE 802.3 - 2000 specification
 - Full- or half-duplex operation
 - CSMA/CD procedures for half duplex*
 - Flow control for full duplex*
 - Jumbo frames support up to 16kB
 - Extensive set of MIB statistical counters*
 - Flexible address filtering
- Control and status registers
 - Configurable 8-, 16-, or 32-bit slave interface
 - Single interrupt line
 - Interrupt mitigation control mechanism
- DMA controller
 - Configurable 8-, 16-, 32-, or 64-bit data bus length
 - Configurable address bus length
 - Big or little endian data byte ordering
 - Scatter/Gather capabilities
 - Programmable burst length
 - Intelligent arbitration between transmit and receive processes
- Descriptor/buffer architecture
 - Descriptor "ring" or "chain" structures
 - Single descriptor points to up to two data buffers
- Low power capabilities
 - Independent clocks for data and control paths
 - Running/Suspended/Stopped modes of operation
 - Clock switching support
- Transmit/Receive dual port RAM interfaces
 - Operate as internal configurable FIFOs
 - Programmable threshold levels

* These features can be removed upon request before delivery to achieve a lower gate count

Functional Description

The MAC1G core consist of the following blocks:

- TC – Transmit Controller. Implements 802.3 transmit operation.
- RC – Receive Controller. Implements 802.3 receive operation.
- BD – Backoff/Deferring. Implements CSMA/CD algorithms for half duplex operation.
- FC – Flow Control. Implements flow control (PAUSE functionality) for full duplex operation.
- SC – Statistical Counters. Implements MIB statistical counters.
- TFIFO – Transmit FIFO. Controls data flow between the MAC and the Transmit Data RAM.
- RFIFO – Receive FIFO. Controls data flow between the MAC and the Receive Data RAM.
- TLSM – Transmit Linked List State Machine. Implements descriptor/buffer architecture.
- RLSM – Receive Linked List State Machine. Implements descriptor/buffer architecture.
- DMA – Direct Memory Access. Provides the data master interface for the MAC.
- CSR – Control and Status Registers. Provides access to the internal registers via slave interface.
- RSTC – Reset Controller. Generates internal reset signals for all clock domains in the design.
- MIIM – Management Interface. Provides access to internal registers of the PHY device.
- TPSM – Transmit Process State Machine. Controls the actual status of the transmit process.
- RPSM – Receive Process State Machine. Controls the actual status of the receive process.

For proper operation of the core the following external components are required:

- Transmit Data RAM – Synchronous dual port RAM working as transmit FIFO memory.
- Receive Data RAM – Synchronous dual port RAM working as receive FIFO memory.
- Address RAM – Synchronous dual port RAM for MAC physical addresses / hash table.
- SC counters RAM – Synchronous RAM for statistical counters.

Customization

Several optional features that may not be required for all applications can be removed from the design upon special request prior to delivery. These are: PHY management interface (MIIM block), Flow control for full duplex (FC block), CSMA/CD procedures for half duplex (BD block), and MIB Statistical counters (SC block).

There are also several controllable generic parameters in the MAC-1G core:

- DATAWIDTH – Data bus width of the data master interface (8/16/32/64, default = 32)
- DATADEPTH – Address bus width of the data master interface (16-32, default = 32)
- CSRWIDTH – Data bus width of the CSR slave interface (8/16/32, default = 32)
- TFIFODEPTH – Transmit FIFO size (up to 64kB, default = 8kB)
- RFIFODEPTH – Receive FIFO size (up to 64kB, default = 16kB)
- TCDEPTH – Number of frames that can reside in the transmit FIFO at the same time (default = 4 frames)
- RCDEPTH – Number of frames that can reside in the receive FIFO at the same time (default = 16 frames)

With source code licenses, these generic parameters can be changed before synthesis. For netlist licenses, changes to these generic parameters must be specified at purchase time and set prior to delivery.

Support

As per the Evaluation License, support for installation and clarification of software functionality is available via email for two weeks after the core is downloaded. A commercial version with full support is also available; contact CAST Sales.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Synplicity version includes:

- HDL RTL source code
- Sophisticated HDL Testbench including that instantiates the MAC-1G core, on chip dual port RAMs, bus/behavioral model of host, bus/behavioral model of shared RAM, bus/behavioral model of PHY device, clock generators, reset generator, and processes that compare your simulation results with the expected results
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide
- Spirit 1.2 IP-XACT model and System Designer files