

CAST

MAC-1G-PCS

Gigabit Ethernet MAC Controller Physical Coding Sublayer

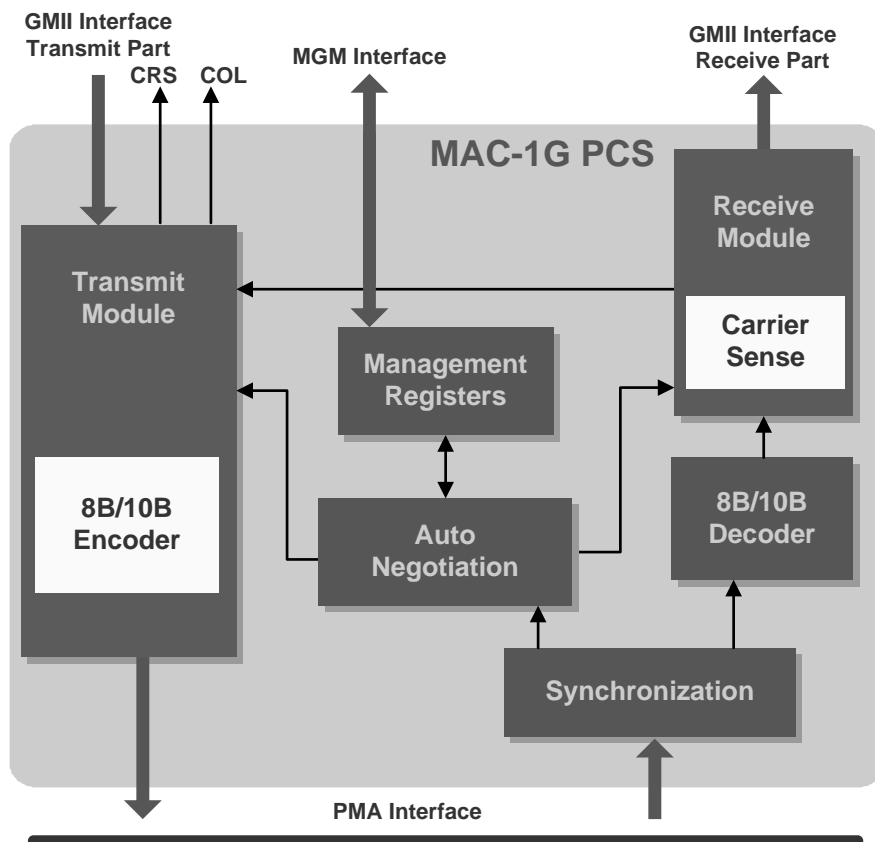
The MAC-1G PCS is an IP core of a 1 Gigabit Physical Coding Sublayer (PCS) that meets all IEEE 802.3-2002 Standard requirements. The MAC-1G PCS provides both PCS interfaces, GMII and PMA. It also features the Management Interface (MGM) for communication with the Station Management (STA).

The MAC-1G PCS has been developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore, scan insertion is straightforward.

Applications

- Ethernet 1000BASE-X
- Repeaters and normal non-repeater devices

Block Diagram



Features

- IEEE 802.3-2002 Standard compliance
- Configurable and monitorable through the Management Interface
- 1000BASE-X Auto-Negotiation process support for information data exchange with a link partner
- 8B-10B Data Encoder/Decoder
- Synchronization Module
- MAC frames encapsulation/de-encapsulation
- Data transmitting/receiving
- Carrier-extension transmitting/receiving
- Idle ordered sets for transmitting/receiving
- Full and half duplex mode support
- Standard Register Set
- PHY loopback mode support with MGM write control register command

Benefits

- Possibility for FPGA implementation with 8B-10B Data Encoder/Decoder located in built-in memory blocks
- Perfect for integrating an Ethernet MAC controller with an optical transceiver through Physical Medium Attachment (PMA) sublayer

Functional Description

The MAC-1G PCS IP core is partitioned into modules as shown in the figure above and described below.

Transmit Module

This provides Ethernet MAC data packets encapsulation and de-encapsulation and sends them to the PMA, as well as generates code-groups based upon the signals delivered from GMII. GMII data octets are converted into the ordered sets according to the state diagram of IEEE 802.3-2002. The module provides continuous fill pattern during inter-packet gaps to establish and maintain clock synchronization. It also supports the Auto-Negotiation process.

Receive Module

This component recognizes data and special code-groups received from the PMA, as well as detects and interprets ordered-sets sent by the link partner according to the state diagram of IEEE 802.3-2002. It also generates appropriate signals on the GMII Interface.

8B/10B Encoder

The module encodes 8-bit data and special groups into 10-bit code-groups depending on the current running disparity. It counts running disparity based upon last encoded code-group and ensures DC balanced bit-stream and high transition density to facilitate clock recovery.

Carrier Sense

This provides detection of a carrier in a received data. This is used for detection of valid data transmission and crs and col signals generation.

Auto – Negotiation Module

This component sets the working mode for the Transmit Module by informing transmit logic to either transmit normal idles interspersed with data packets from Ethernet MAC or to reconfigure the link by the auto-negotiation (AN) process. It is also responsible for setting the status registers and ability advertisement of link partner registers for use by the Station Management (STA), as well as for reading/writing configuration registers of the Management Registers unit. The module supports management registers from 0 to 6 and register number 15 (basic set plus some from extended set).

Synchronization Module

This accepts code groups received from the PMA and conveys them to the Receive Module. It checks if received code groups are valid and informs AN module about lost or obtained synchronization. This information is further used to establish appropriate work mode.

8B/10B Decoder

The Decoder provides decoding of 10-bit data and special groups into 8-bit code-groups and supports invalid or faulty code groups detection.

Management Registers Module

This provides the Base Register Set, which is a set of six dedicated management registers, as well as the MGM Interface for communicating with Station Management (STA). The module implements a mechanism to read/write status and configuration registers. Management Registers also communicate with the Auto-Negotiation Module to ensure data and ordered sets exchange between the PCS and the Station Management.

Performance

The PCS works with the standard 125MHz clock on GMII interface and the 2.5MHz clock on MGM interface.

The PCS introduces the following delays:

Event	Delay (bit time)	Input Timing Reference	Output Timing Reference
TX_EN=1 to tx_code_group	32	rising edge of gtx_clk	/S/ code-group
rx_code_group to CRS assert	48	rising edge of clk_pma_rx for /S/	
rx_code_group to CRS deassert	32	rising edge of clk_pma_rx for /K28.5/	
rx_code_group to COL assert	32	rising edge of clk_pma_rx for /S/	
rx_code_group to COL deassert	16	rising edge of clk_pma_rx for /K28.5/	
TX_EN=1 to CRS assert	16	rising edge of gtx_clk	
TX_EN=1 to CRS deassert	16	rising edge of gtx_clk	
rx_code_group to RX_DV deassert	48	rising edge of clk_pma_rx for /T/	rising edge of clk_pma_rx when RX_DV goes low

Implementation Results

MAC-1G-PCS reference designs have been evaluated in a variety of technologies. The following is a sample result using optimization for speed.

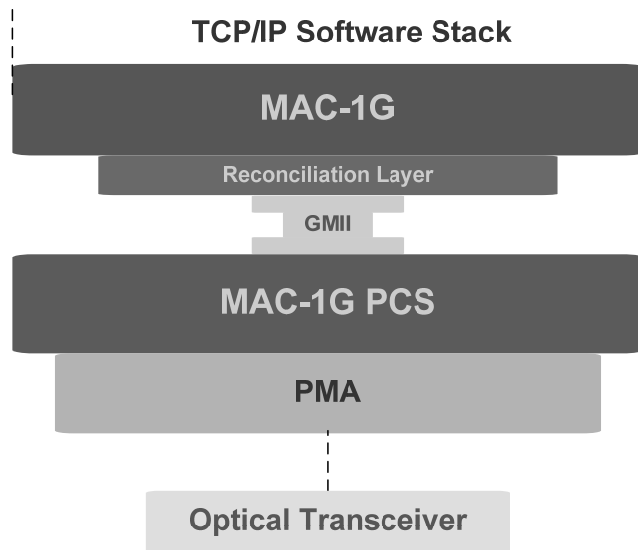
ASIC Technology	Area	Speed
UMC 0.18µm	7700 gates	171 MHz

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Example Application

The following figure presents typical application of the MAC-1G PCS IP core.



The MAC-1G PCS provides a sublayer needed for establishing Gigabit Ethernet communication over fiber-optic cable. The common use of such an optical connection is implementing TCP/IP stack for connecting embedded systems with the computer network.

Configurability

The following parameters allow adjustment of the MAC-1G PCS core to requirements of target application or technology:

- The Auto-Negotiation process enable/disable
- Base page configuration according to the standards

Additional parts of the system or modifications of the IP core may be developed by Evatronix according to the user's application.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

The trial ATPG coverage figures met the requirements and reached level of over 99% for statement, branch and condition.

Related Products

MAC-1G: the most feature-rich controller in the CAST MAC family. It operates at 10/100/1000 Mbps speed modes and contains the integrated descriptor based DMA. Its features include MII PHY management, Flow Control, and a full set of Statistical Counters.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- Sophisticated self-checking HDL Testbench
- Simulation scripts, vectors, expected results, and comparison utility
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Options

Typically the core is delivered as HDL source code for ASIC implementations. The following options may be ordered according to the user's requirements:

Evaluation system including:

- MEMEC VIRTEX-II PRO FF1152 Development Board
- Two optical GbE SFP modules
- MCS file with implementation of the MicroBlaze™ microcontroller with integrated MAC-1G PCS
- Software webserver for MicroBlaze™ with a simple web page