

# CAST

## MAC-1G-L

### Lite 1-Gigabit Ethernet Media Access Controller Core

The MAC-1G-L implements a lean, gigabit-speed LAN controller using the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by the IEEE 802.3 standard for media access control over Ethernet.

The core uses a standard Gigabit Media Independent Interface (GMII). It provides full-duplex operation for 10/100/1000 Mbit/s transmission modes, and if desired half-duplex operation for 10/100 Mbit/s modes. Configurable features allow tailoring of the data interface bus width (8-, 16-, or 32-bit), the transmit and receive FIFO sizes (64B to 64kB).

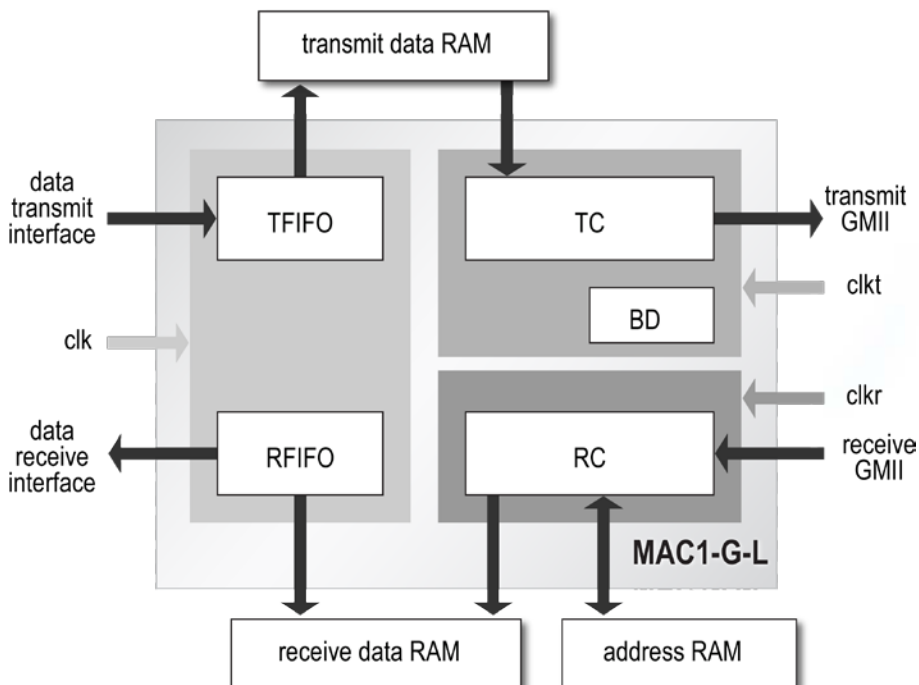
The MAC-1G-L is designed for easy reuse in ASICs and FPGAs. The design is strictly synchronous with positive-edge clocking, no internal tri-states and with a synchronous reset. Scan insertion is straightforward. The efficient uses little silicon area, using for example under 12,500 gates in an ASIC .18 $\mu$ m process. Thorough verification has included FPGA implementations and testing in prototype systems.

### Applications

The MAC-1G-L can be used in a variety of LAN controller applications including:

- Network Interface Cards (NICs)
- Routers, switching hubs
- Systems On Chip (SOCs)

### Block Diagram



### Features

- Network interface features
  - Supports data transfer rates of 1 Gb/s and 10/100 Mb/s
  - Gigabit Media Independent Interface (GMII)
- Data link layer functionality
  - Meets IEEE 802.3 CSMA/CD standard
  - Full duplex operation for 10/100/1000 Mbit/s modes
  - Half duplex operation for 10/100 Mb/s modes
- Flexible address filtering
  - External RAM for storing MAC addresses
  - Up to 16 physical addresses
  - 512-bit hash table for multi-cast addresses
- Transmit/Receive dual port RAM interfaces
  - Operate as internal configurable FIFOs
  - Programmable threshold levels
  - "Store and forward" functionality

### Configurable Features

- Data interface bus width: 8-, 16-, or 32-bit
- Transmit FIFO size: 64B to 64kB
- Receive FIFO size: 64B to 64kB
- Backoff/deferring controller can be easily removed for lower gate count if the half duplex operation is not required.

### Options

- RMII - Reduced MII interface instead of standard MII
- SMII - Serial MII interface instead of standard MII

## Functional Description

### TC – Transmit Controller

Implements the 802.3 transmit operation. From the network side it uses the standard 802.3 GMII interface for an external PHY device, and it operates synchronously with the `clkt` clock from the GMII interface.

### BD – Backoff/Deferring (removable)

Implements the 802.3 half duplex operation, and can be omitted if half-duplex is not needed. It operates synchronously with the `clkt` clock from the GMII interface.

### RC – Receive Controller

Implements the 802.3 receive operation. From the network side it uses the standard 802.3 GMII interface for an external PHY device. It operates synchronously with the `clkr` clock from the GMII interface.

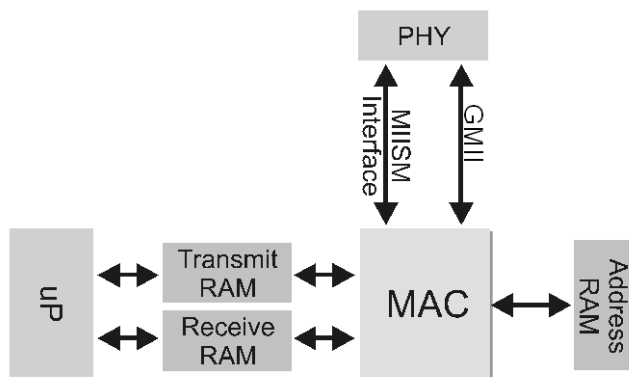
### TFIFO – Transmit FIFO

Buffers data prepared for transmission by the MAC-1G-L. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: `TFIFODEPTH` defines the total FIFO size, and `TCDEPTH` defines the maximum number of frames that can reside in the transmit FIFO at the same time. The TFIFO controller operates synchronously with the `clk` host-side clock.

### RFIFO – Receive FIFO

Buffers data received by the MAC-1G-L. It provides an interface for the external dual-port RAM working as FIFO memory. The FIFO size can be configured by the generic parameters of the core: `RFIFODEPTH` defines the total FIFO size, and `RCDEPTH` defines the maximum number of frames that can reside in the receive FIFO at the same time. The RFIFO controller operates synchronously with the `clk` host-side clock.

## Example Application



The MAC-1G-L Controller is used to implement 10, 100 and 1000 Mbit/s Ethernet networks interface in a customer system. The example application system consists of the microcontroller and the MAC-1G-L module. The host transmits and receives frames through the FIFO memories interfaces (transmit and receive RAMs). The operation mode of the Ethernet controller is provided via set of configuration pins that can be mapped into microcontroller memory/port(s) or hard-coded to the one desired configuration.

## Implementation Results

MAC-1G-L reference designs have been evaluated in a variety of technologies. The following are sample ASIC results with optimization for speed.

ASIC Technology	Approx. Area	MII/GMII Speed	Host Side Speed
UMC 0.18um	12,430 gates	>125 MHz	> 125 MHz
TSMC 65nm LP	29,240 gates	> 125 MHz	>125MHz

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has been implemented in FPGAs, and successfully evaluated in prototype systems.

## Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- An example MAC-1G-L\_CHIP implementation, which illustrates how to build and connect memories and port modules
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including detailed specifications and a system integration guide