LLEMAC-1G

Low-Latency 10/100/1000 Ethernet MAC

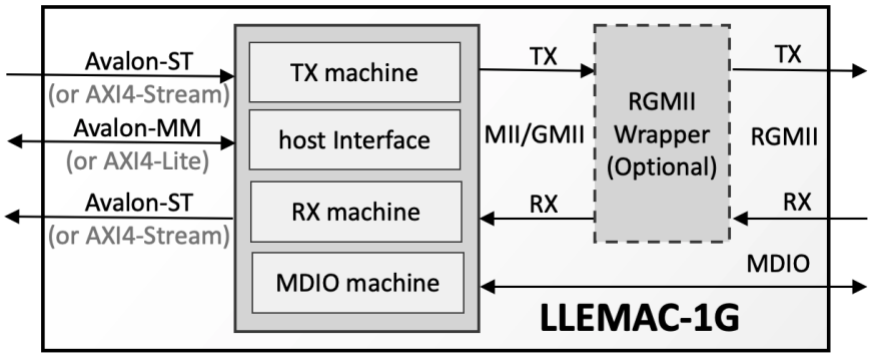
The LLEMAC-1G implements an Ethernet Media Access Controller compatible with the 10/100 Mbps IEEE 802.3 and 1Gbps IEEE 802.3-2002 specifications. Featuring extremely low egress and ingress latency, the core is ideal for the implementation of TSN Ethernet nodes, live streaming and other devices requiring minimum latency in the reception and transition of Ethernet frames.

The core supports full-duplex operation, supports jumbo frames, provides statistics counters, and it is easy to integrate and implement. The LLEMAC-1G exchanges data with the host system via byte-wide streaming interfaces, and connects to the external PHY via an MII, GMII, or RGMII interface. An independently clocked, 32-bit wide memory mapped-interface provides access to the core's control and status registers. The default core interfaces comply with the Avalon standard, but AMBA™ AXI4 can also be made available upon request.

The LLEMAC-1G is available in two versions: Normal, and Safety-Enhanced. The Safety-Enhanced version implements clock activity monitors and uses spatial redundancy for protecting the inner logic of the core. The deliverables for this version include a Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA), and the ISO-26262 "ASIL-D Ready" certificate, issued by SGS-TÜV Saar GmbH.

The core is provided in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including an extensive testbench, sample scripts, and comprehensive documentation.

Block Diagram



Implementation Results

The provided figures do not represent the higher speed or smaller area for the core. Area, power and speed depend on configuration, optimizations, process, and libraries. Contact CAST to get characterization data for your target configuration and technology.

Core Configuration	Technology	Frequency (MHz)	Eq. NAND2 Gates
Normal/Default	TSMC 16nm	125 MHz	6,540
Normal/Default	TSMC 28nm	125 MHz	6,170
Normal/Default	TSMC 40nm	125 MHz	7,915

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

Low-Latency Ethernet MAC

- Supports IEEE 802.3
- Enables high-precision synchronization in TSN networks
  - Egress latency: 10 Tx clock cycles
  - Ingress latency: 6 Rx clock cycles
- Full duplex point-to-point links

Easy System Integration

- Autonomous operation, requires no host assistance once programmed
- Host Interfaces
  - Avalon-MM: memory mapped, or optionally AXI4-Lite
  - Avalon-ST: stream, or optionally AXI4-Stream
- PHY Interfaces
  - Media Independent Interface (MII) for 10/100Mbps
  - Gigabit Media Independent Interface (GMII) for 1Gbps
  - Reduced Gigabit Media Independent Interface (RGMII) for 10/100/1000 Mbps
  - MDIO interface for PHY configuration and management

Safety-Enhanced Version (optional)

- Certified ISO-26262 "ASIL-D Ready"
- Spatial redundancy for inner logic protection
- Clock activity monitoring

Deliverables

- Source code VHDL or Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Comprehensive documentation