

CAST



I2C

Master/Slave Bus Controller Core

The I2C core implements a serial interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus.

The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register (i2csta) reflects the status of I2C Bus Controller and the I2C bus.

The I2C is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Applications

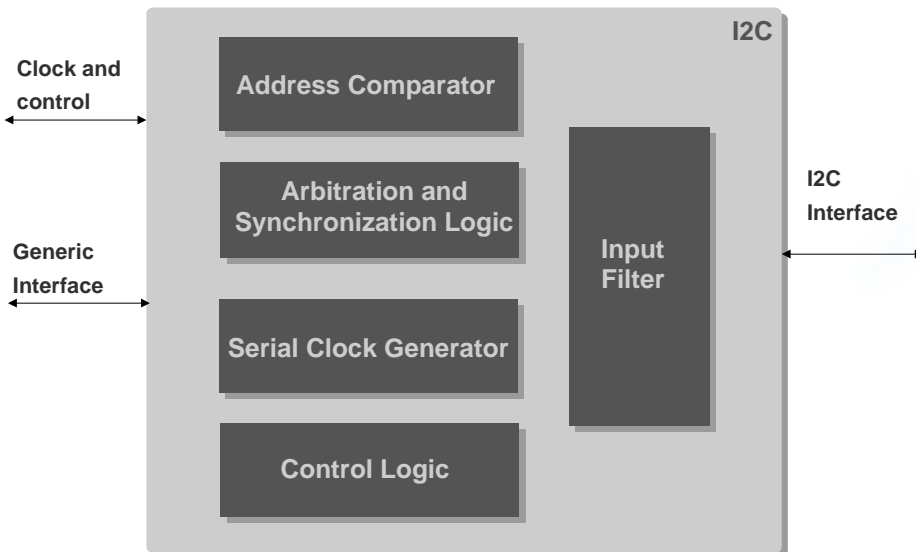
The I2C can be utilized for a variety of serial interface applications including:

- Embedded microcontroller systems
- Communication systems

Benefits

- I2C provides a convenient interface to I2C bus – the de facto world standard in a broad range of applications
- I2C uses only 2 wires to connect to virtually an unlimited number of devices, therefore minimizing interconnections and usage of IC pins in the user application
- I2C standard implements a simple and efficient bus which does not require additional logic such as address decoders or arbiters

Block Diagram



Features

- Master Transmitter Mode — Serial data output through SDA while SCL outputs the serial clock.
- Master Receiver Mode — Serial data is received via SDA while SCL outputs the serial clock.
- Slave Receiver Mode — Serial data and the serial clock are received through SDA and SCL.
- Slave Transmitter Mode — Serial data is transmitted via SDA while the serial clock is input through SCL.
- Data transfers up to 100 Kbps in standard mode and up to 400 Kbps in fast-mode.
- Bi-directional data transfer.
- Own address and General Call address detection.
- 7-bit addressing format.
- Fixed data width of 8 bits.
- Data transfer in multiples of bytes.
- One-byte write and read buffer.

Functional Description

The I2C core is partitioned into modules as shown in the Block Diagram and described below.

Arbitration and synchronization logic

In the master mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I2C bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost and the I2C immediately changes from master transmitter to slave receiver. The synchronization logic will synchronize the serial clock generator with the clock pulses on the SCL line from another device.

Serial clock generator

This programmable clock pulse generator provides the SCL clock pulses when the I2C is in the master mode. The clock generator is switched off when the I2C is in a slave mode.

Control logic

The control logic generates the control signals for serial byte handling.

Input filter

Input signals are synchronized with the internal clock (clk), and spikes shorter than three oscillator periods are filtered out.

Address comparator

The comparator compares the received 7-bit slave address with its own slave address. It also compares the first received 8-bit byte with the general call address (00H). If equality is found, the appropriate status bits are set and an interrupt is requested.

Core Modifications

The I2C core can be modified to change the serial transmission bit rate. Please contact CAST, Inc. directly for any required modifications.

Configurability

- Hardware configurability features:
 - Glitch register: configurable glitch removal length from both clock and data lines
- Runtime configuration features:
 - Own address
 - I2C clock generation:
 - From division of system clock
 - From external clock generator
 - Toggle general call address accept

Implementation Results

I2C reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with Slices optimized for speed, assuming all core I/O is routed off-chip.

Supported Family	Slices	BRAM	IOB	Fmax (MHz)	ISE Version
Spartan-3E 3S500E-5	262	-	24	143	12.2i
Spartan-6 6SLX4-3	102	-	24	202	12.2i
Virtex-5 5VLX30-3	135	-	24	258	12.2i
Virtex-6 6VLX75T-3	81	-	24	297	12.2i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Testbench (self checking)
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Products

I2C-HS – is an I2C Bus Controller which provides a serial interface that meets the Philips I2C bus specification v.2.1, compliant with PVCI (Peripheral Virtual Component Interface) or AMBA[®] AHB interfaces.