The I2C-SMBUS core implements a serial interface controller for the Inter-Integrated Circuit (I2C) bus and the System Management Bus (SMBus).

The core can be programmed to operate either as a bus master or a slave, and it is easy to program and integrate. An arbitration mechanism allows operation in a multiple master bus and the SMBus provisioned clock synchronization mechanism allows fast-master/slow-slave communication. Furthermore, the core detects timeout and errors to prevent bus deadlocks, and can filter out glitches on the serial line. The control, status, and data registers of the I2C-SMBUS core are accessible via an AMBA APB or a generic memory mapped interface.

The I2C-SMBUS is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design uses rising-edge-triggered flip-flops only with the reset type (i.e. asynchronous and/or synchronous) being configurable at synthesis time. Furthermore, the core does not use tri-states; therefore scan insertion is straightforward.

Applications
The I2C-SMBUS can manage the communication of a host processor with peripherals such as sensors, smart battery subsystems, analog front ends, analog-to-digital and digital to analog converters, and display controllers.

Block Diagram

Implementation Results
I2C-SMBUS core reference designs have been evaluated in a variety of technologies. The following are sample implementation results.

<table>
<thead>
<tr>
<th>Technology</th>
<th>I2C-SMBUS (w/o Timer) Area</th>
<th>Timer Area</th>
<th>Core/Bus Clock Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 90nm process</td>
<td>1,500 gates</td>
<td>600 gates</td>
<td>50 MHz</td>
</tr>
<tr>
<td>TSMC 40nm process</td>
<td>1,750 gates</td>
<td>700 gates</td>
<td>50 MHz</td>
</tr>
</tbody>
</table>

Support
The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.