I2C-SMBUS
I2C & SMBUS Controller Megafunction

The I2C-SMBUS megafunction implements a serial interface controller for the Inter-
egrated Circuit (I2C) bus and the System Management Bus (SMBUS).

The megafunction can be programmed to operate either as a bus master or slave, and
it is easy to program and integrate. An arbitration mechanism allows operation in a mul-
tiple master bus and the SMBUS provisioned clock synchronization mechanism allows
fast-master / slow-slave communication. Furthermore, the megafunction detects timeout
events to prevent from bus deadlocks, and can filter-out glitches on the serial line.
The control, status and data registers of the I2C-SMBUS megafunction are accessible
via an AMBA APB or a generic memory mapped interface.

The I2C-SMBUS is a microcode-free design developed for reuse in ASIC and FPGA
implementations. The design uses rising-edge-triggered flip-flops only with the reset
type (i.e. asynchronous and/or synchronous) being configurable at synthesis time. Fur-
thermore, the megafunction does not use tri-states; therefore scan insertion is
straightforward.

Applications

The I2C-SMBUS can be utilized for the communication of a host processor with periph-
erals such as sensors, smart battery subsystems, analog front ends, analog-to-digital
and digital to analog converters, and control of displays.

Block Diagram

Implementation Results

I2C-SMBUS megafunction reference designs have been evaluated in a variety of tech-
nologies. The following are sample implementation results on Altera FPGAs for the
megafunction configured with an APB interface and the optional timer instantiated.

<table>
<thead>
<tr>
<th>Family</th>
<th>Device</th>
<th>Logic</th>
<th>Memory Bits</th>
<th>Clock Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone IV GX</td>
<td>EP4CGX1SBF14C6</td>
<td>598 LEs</td>
<td>0</td>
<td>175 MHz</td>
</tr>
<tr>
<td>Cyclone V</td>
<td>5CEFA2F2317</td>
<td>281 ALMs</td>
<td>0</td>
<td>175 MHz</td>
</tr>
</tbody>
</table>

Support

The megafunction as delivered is warranted against defects for ninety days from pur-
chase. Thirty days of phone and email technical support are included, starting with the
first interaction. Additional maintenance and support options are available.

Features

Standards Compliance
- Phillips I2C
- SMBUS Ver 1.0

Operation Modes
- Master Transmitter Mode
- Master Receiver Mode
- Slave Receiver Mode
- Slave Transmitter Mode

Functionality
- 7 Bits Addressing
- Byte-wide transfers
- Bus Arbitration
- Clock signal (SCL) generation (in master mode) and data synchronization
- START/STOP Timing detection and generation
- Timeout/Bus error detection
- Clock-Low Extension to allow fast-master slow-slave communication
- Configurable glitches filter for clock and data serial lines
- Bus-status reporting

Interfaces
- I2C –SMBus
  - A pair of unidirectional signals for SCL and SDA
  - Control for the serial line buffers / drivers
- Host
  - 32-bit APB or 8-bit generic (8051-like) for register ac-
    cess
  - Interrupt line
- Clocks
  - Megafunction operates on the host-interface clock
  - Reference clock signals used to generate the serial clock
    (SCL)

Deliverables
- RTL source code or targeted FPGA netlist
- Test-bench
- Sample simulation and synthesis script
- Extensive documentation
- Sample SMBUS software driver