

# CAST

## I2C-M I2C Bus Master Controller Core

### Features

- I2C Master Transmit and Master Receive Modes, suitable for uni-master buses
- I2C Bus Speeds
  - Standard-mode (Sm): up to 100 Kbps
  - Fast-mode (Fm): up to 400 Kbps
  - Fast-mode Plus (Fm+): up to 1Mbps
  - High-Speed mode (Hs): up to 3.4 Mbps
  - Unidirectional Ultra Fast Speed (UFm): up to 5 Mbps
- 7- and 10-bit slave address
- Acknowledge/Not Acknowledge cycle by slave (required for all modes but UFm) or master (required by UFm)
- Clock Stretching Support
- Suitable for implementing I2C variants such as SMBUS and PMBUS

### Easy to Use

- Control and monitor via 8-bit-wide control status registers
- Compact set of commands control I2C Transactions
- Rich set of maskable interrupts
- Command and read FIFOs for lower host overhead
- Programmable clock divider derives serial clock from bus clock or externally provided clock
- Low-Level Driver in C

### Configurable

- Host Interface options include APB (default), AHB, Wishbone, and 8051-SFR
- Adjustable Receive Data and Command FIFO sizes

Implements an Inter-Integrated Circuit (I2C) Bus master controller that meets the Phillips I2C, version 4.0 specification for single master I2C buses.

The I2C-M allows dynamic control of the serial clock frequency, and the I2C bus speed is only limited by the external bus driver capabilities and the frequency used to clock the core. It supports a 7- or 10-bit slave address and allows the Acknowledge cycle to be controlled by either the slave or the master. This enables operation in all bus speed modes provisioned by version 4.0 of the standard, including the unidirectional Ultra Fast Speed. Furthermore, the core is suitable for implementing the master node for I2C-based protocols, such as SMBUS, PMBUS and VESA Display Data Channel (DDC).

Under its default configuration, the I2C-M provides access to its 8-bit-wide status and control registers via an APB-slave port. Alternatively, the core can be equipped with an AHB-slave, Wishbone-slave, or generic microcontroller interface.

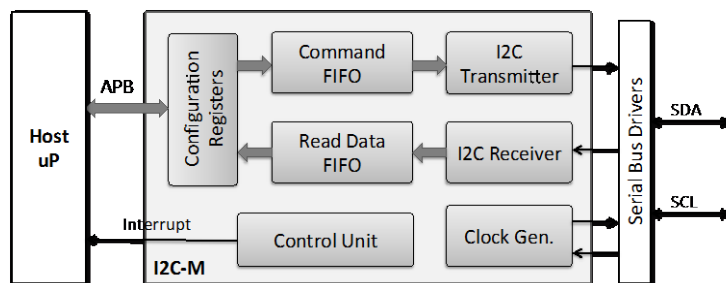
Controlled by a compact and comprehensive set of commands and accompanied by a low-level C-driver, the I2C-M core enables easy and rapid development of over-I2C, or I2C-like protocols in user applications. The configurable size FIFOs for read-data and commands and a rich set of interrupts help reduce host processor overhead and interaction.

The I2C-M is production-proven in ASIC and FPGA technologies.

### Applications

The I2C-M enables microcontrollers to interface I2C peripherals such as EEPROM, A/D and D/A Converters, sensors, smart cards, and LCD and LED drivers.

### Block Diagram



### Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### Deliverables

The core is available in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including an extensive testbench, comprehensive documentation and a low-level device driver.