

CAST

I2C-HS

Master/Slave Bus Controller Core

The I2C-HS core implements a serial interface that meets the Philips I2C Bus® specification version 2.1. It is compliant with the PVICI (Peripheral Virtual Component Interface) standard which is an open standard for SoC On-Chip Bus.

The I2C-HS is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

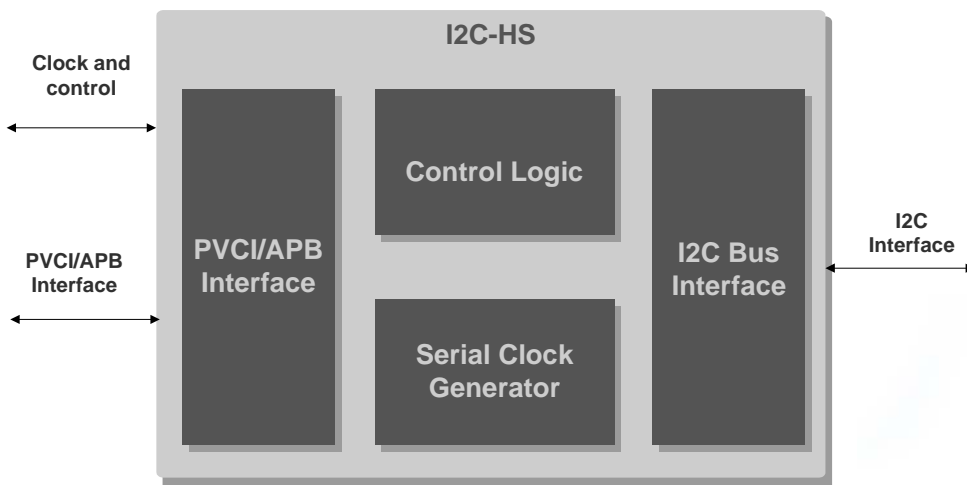
Applications

- The I2C can be utilized for a variety of serial interface applications.

Benefits

- I2C provides a convenient interface to I2C bus – the de facto world standard in a broad range of applications
- I2C uses only 2 wires to connect to virtually an unlimited number of devices, therefore minimizing interconnections and usage of IC pins in the user application
- I2C standard implements a simple and efficient bus which does not require additional logic such as address decoders or arbiters

Block Diagram



Features

- The I2C Bus uses two wires to transfer information between devices connected to the bus: SCL (serial clock line) and SDA (serial data line)
- Compliant to version 2.1 of the I2C Bus standard
- PVICI standard compliant (OCB 2 2.0)
- Data transfers up to 100 Kbps in standard mode, up to 400 Kbps in fast-mode, and up to 3.4 Mbps in high-speed mode
- Master Transmitter Mode — Serial data output through SDA while SCL outputs the serial clock
 - Master Receiver Mode — Serial data is received via SDA while SCL outputs the serial clock
 - Slave Receiver Mode — Serial data and the serial clock are received through SDA and SCL
 - Slave Transmitter Mode — Serial data is transmitted via SDA while the serial clock is input through SCL
- Mixed-speed bus system configuration support
- Multimaster Mode
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Functional description

The I2C-HS core is partitioned into modules as shown in figure above and described below.

I2C Bus Interface

Handles all bit operations directly at I2C bus level. In slave mode, it detects start and stop conditions, acknowledge, operation direction, etc. In master mode, it controls state of *scl* and *sda* lines according to requests from the PSCI initiator.

Control logic

Handles all byte-level logic that the core must provide in order to comply with the I2C protocol.

PSCI/AHB Interface Controller

Handles information exchange with either the PSCI or AHB initiator. On the *val* signal it receives all necessary data and asserts the *ack* signal to tell initiator that the data was accepted.

Serial clock generator

This programmable clock pulse generator provides the SCL clock pulses when the I2C-HS is in the master mode. The clock generator is switched off when I2C-HS is in a slave mode.

Implementation Results

I2C-HS reference designs have been evaluated in a variety of technologies. The following are sample ASIC results optimized with a clock constraint of 100 MHz.

ASIC Technology	Approx. Area	Frequency
TSMC 0.18 μ process	3900 gates	131 MHz
TSMC 0.13 μ process	3800 gates	143 MHz
TSMC 90nm process	3600 gates	214 MHz

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

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Configurability

- Hardware configurability features:
 - 10-bit address disable
- Runtime configuration features:
 - Own address
 - I2C clock generation:
 - From division of system clock
 - From external clock generator

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) that instantiates the core, clock generator, bus/behavioral model of the I2C-HS, bus/behavior model for the 8051 host, and the process that compares the simulation results with the expected results
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Products

I2C – is an I2C Bus Controller which provides a serial interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The core is available with either a generic or AMBA[®] AHB interface.