DPTx-CTRL
DisplayPort Transmitter Controller

Implements a DisplayPort transmitter compatible with the latest versions of the VESA DisplayPort (DP) Standard and the companion Embedded DisplayPort (eDP) Standard. The core supports all link functionality including the Main Link, Secondary Channel, and AUX Channel protocols. It also optionally supports the HDCP on DisplayPort standard for data encryption.

The core is designed for easy integration, providing industry-standard interfaces and including required software. It uses a streaming-capable VS/HS video input capable of one or two pixels per cycle, I2S and optionally S/PDIF audio interfaces, and AMBA/APB for the host interface. The PHY interface is designed to connect with and has been verified with most third party interface cores.

The core’s deliverables include a standard-compliant link policy maker and a fully documented API. An available FPGA based reference design system provides a complete development environment to facilitate core evaluation and software development. Integration services are available to deliver a complete DisplayPort solution optimized for the customer’s target technology.

The silicon-proven core has been produced in FPGA and several ASIC technology nodes, and is available in RTL source code or FPGA targeted netlist formats.

Applications
Display Port and embedded Display port are used as external as well as internal (embedded) display interfaces in applications such as:

- Notebooks
- Ultrabooks
- Tablets
- Graphic Cards
- PC Motherboards
- Blu-Ray Disc Players

Block Diagram

Features
Overview
- DisplayPort 1.1a / 1.2a
- Embedded DisplayPort (eDP) 1.4
- Up to four lanes in the main link
- Secondary audio channel
- 1Mbps AUX channel
- HDCP support (optional)
- Single Stream Transport
- Multi Stream Transport (opt.)
- Enhanced 3D Video Transport
- Multiple link rate support
  - 5.4Gbps, 4.23 Gbps, 3.24Gbps, 2.7Gbps, 2.43Gbps, 2.16Gbps or 1.62Gbps

Audio Support
- Up to eight channels
- 192MHz Max. Sampling Rate
- I2S and SPDIF (optional) interfaces

Video Support
- Up to 48 bits per pixel
- 422 and 444 support
- YCrCb to RGB conversion
- Interlaced video support
- 3D Video support
- Standard VS/HS interface

eDP Features
- Panel Shelf-Refresh
- Panel Shelf Test Indicator
- Display Panel Control Protocol
- Gamma Correction
- Dynamic Refresh Rate
- Dithering and 6-bit FRC
- Fast Link Training
- Alternate Framing
- Alternative Scrambler Reset
- Advanced Link Power Management
- Display Stream Compression
- Multi-Touch Over AUX
- Increased Voltage Swing Range
- Four Additional Link Rates

Easy Integration
- Industry-Standard Interfaces
- Link Policy Maker Software & API
- FPGA reference design

Maturity
- Third-generation design
- Production proven with different 3rd party PHYs in a wide-range of technologies

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Implementation Results

The DPTx-CTRL core was developed using best-in-class design principles and is very efficient in resource usage. The core synthesizes to about 65k gates and 3Kbits of memory. Please contact CAST for detailed area and timing results for any specific technology you require.

FPGA Development & Evaluation Platform

The available Development & Evaluation Platform implements this core in an FPGA, allowing quick and cost-effective evaluation and early software prototyping.

The ready-to-run platform includes a 32-bit host processor capable of running custom applications, a Display Controller and other built-in interfaces, and a peripherals suite running a flash-based ROM monitor that loads at power-up.

Using the integrated Compact Flash system, custom application software can be loaded onto the system for early development. The video output system uses a standard daughter card that includes the DisplayPort output connector. The DisplayPort output can drive monitors up to and including 1900x1200 in resolution.

The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.

Support

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The DPTx-CTRL has been rigorously verified using random and directed testing covering. The core has been validated against the DisplayPort compliance test suite (results available upon request). Extensive interoperability testing has also been conducted using a wide variety of shipping products. The core has been silicon- and production-proven.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- Reference driver, API and Link Policy Maker in C
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and timing constraints simulation summary
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including a fully documented API, and functional specification.