DPRx-CTRL
DisplayPort Receiver Controller

Implements a DisplayPort receiver compatible with the latest versions of the VESA DisplayPort (DP) Standard and the companion Embedded DisplayPort (eDP) Standard. The core supports all link functionality including the Main Link, Secondary Channel, and AUX Channel protocols. It also optionally supports the HDCP on DisplayPort standard for data encryption.

The core is designed for easy integration, providing industry-standard interfaces and including required software. It uses a streaming-capable VS/HS output interface for video, I2S and optionally S/PDIF audio interfaces, and AMBA/APB for the host interface. The PHY interface is designed to connect with and has been verified with most third-party interface cores.

The included reference software implements a low-complexity driver and a fully-documented API. An available FPGA based reference design system provides a complete development environment to facilitate core evaluation and software development. Integration services are available to deliver a complete DisplayPort solution optimized for the customer’s target technology.

The silicon-proven core has been produced in FPGAs and several ASIC technology nodes, and is available in RTL source code or targeted FPGA netlist formats.

Applications
DisplayPort and Embedded DisplayPort transmitters are used as external and internal (embedded) display interfaces in applications such as:

- Computer Displays
- Graphic Cards
- All-in-one Desktops
- Ultrabooks
- Tablets
- Notebooks

Block Diagram

Features

Overview
- DisplayPort 1.1a/1.2a, including MST & HBR2
- Embedded DisplayPort (eDP) 1.3
- Up to four lanes in the main link
- Secondary audio channel
- 1Mbps AUX channel
- HDCP (optional)
- Single Stream Transport
- Enhanced 3D Video Transport
- Multiple link rate support 5.4Gbps, 2.7Gbps or 1.62Gbps

Audio Support
- Up to eight channels
- 192MHz Max. Sampling Rate
- Multiple I2S and SPDIF (optional) interfaces

Video Support
- Up to 48bits per pixel
- 422 and 444 support
- YCrCb to RGB conversion
- Interlaced video support
- 3D Video support
- Standard VS/HS interface

eDP Features
- Panel Shelf-Refresh
- Panel Shelf Test Indicator
- Display Panel Control Protocol
- Gamma Correction
- Dynamic Refresh Rate
- Dithering and 6bit FRC
- Fast Link Training
- Alternate Framing
- Alternate Scrambler Reset

Easy Integration
- Industry-Standard Interfaces
- Minimal configuration overhead for the host processor
- Included Reference Software
  - Low complexity driver
  - Sample configuration
  - Fully documented API
- Industry-Standard Interfaces
- FPGA reference design

Maturity
- Third-generation design
- Production proven with different 3rd party PHYs in a wide-range of technologies
Implementation Results

The DPRx-CTRL core was developed using best-in-class design principles and is very efficient in resource usage. The core synthesizes to about 60k gates and 1.5Kbits of memory. Please contact CAST for detailed area and timing results for any specific technology you require.

FPGA Development & Evaluation Platform

The available Development & Evaluation Platform implements this core in an FPGA, allowing quick and cost-effective evaluation and early software prototyping.

The ready-to-run platform includes a 32-bit host processor capable of running custom applications, a DVI Controller and other built-in interfaces, and a peripherals suite running a flash-based ROM monitor that loads at power-up.

Using the integrated Compact Flash system, custom application software can be loaded onto the system for early development. The video input system uses a standard daughter card that includes the DisplayPort input connector. The DVI output can drive monitors up to 1900x1200 in resolution.

The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.

Support

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The DPRx-CTRL has been rigorously verified using random and directed testing covering. The core has been validated against the DisplayPort compliance test suite (results available upon request). Extensive interoperability testing has also been conducted using a wide variety of shipping products. The core has been silicon- and production-proven.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- Reference driver, and API in C
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and timing constraints simulation summary
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including a fully documented API, and functional specification.