

CAST

ALTERA®

CAN Bus Controller Megafunction

The development of increasingly complex microsystems requires the usage of powerful field bus systems for distributed real-time networks. The CAN protocol has a wide acceptance in the field of serial communication.

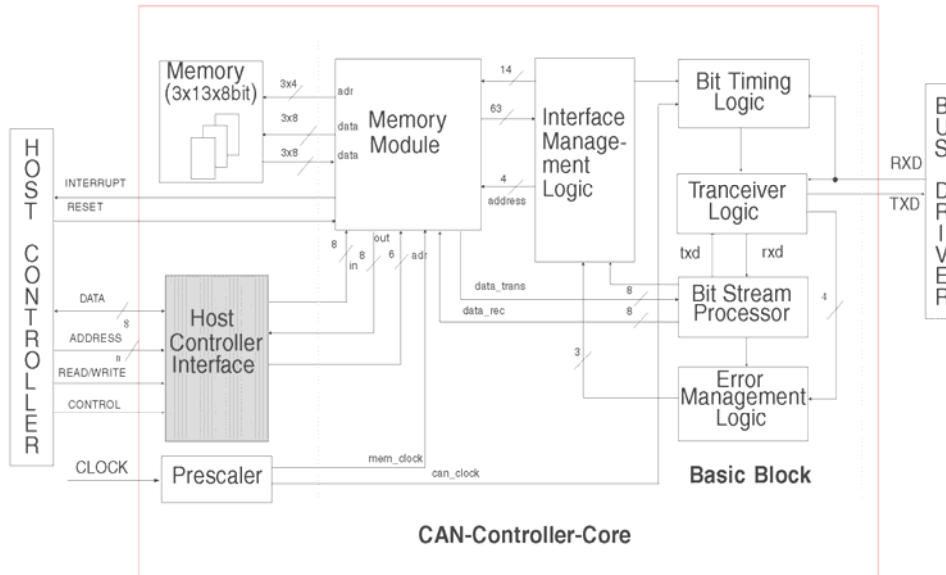
The CAN bus controller megafunction is described at the RTL system level which allows easy targeting of various technologies.

The CAN bus megafunction is founded on the basic CAN principle and meets all constraints of the CAN-specification 2.0B. For buffering of received or transmitted messages, three 13-byte buffers are used. In practice, no overload frames will be generated.

Applications

- Railway
- Automotive
- Industrial

Block Diagram



Features

- Implementation of the Basic CAN specification
- No generated Overload Frames
- Receiving and transmitting of both identifiers (CAN specification 2.0B)
- Programmable data rate up to 1 mbps
- Programmable baud rate prescaler (up to 1/30)
- Application-specific interface to the host-controller
- Link to commercial bus drivers (for instance, PCA82C250T by Philips)
- Verified with the Bosch reference model
- The CAN Controller synthesizes to approximate 6500 gates

Functional Description

The CAN bus megafunction is founded on the basic CAN principle and meets all constraints of the CAN-specification 2.0B. For buffering of received or transmitted messages, three 13-byte buffers are used. In practice, no overload frames will be generated.

The Control Segment contains all necessary registers for controlling and configuring of the chip. The host controller is able to read and write the memory module as a conventional RAM in memory mapped mode.

The controller interface is interchangeable. All events on the data bus or in the controller are flagged as an interrupt to the host controller. Every interrupt may be enabled or disabled. The controller contains a 27-bit acceptance mask and a 27-bit acceptance code register.

The host controller interface is connected with the memory module by two 8-bit data buses and a 6-bit address bus. This allows for an easy interface exchange when using another host controller.

Implementation Results

CAN reference designs have been evaluated in a variety of technologies. The following are sample results using describe constraints and details for getting results and optimization for speed.

| Supported Family | Utilization | | | Performance |
|------------------------|-------------|--------|-------------|-------------|
| | LEs | Memory | Memory Bits | Fmax |
| Flex EPF10K50E-2 | 1733 | 3 EAB | 384 | 20 MHz |
| Acex EP1K50-1 | 1733 | 3 EAB | 384 | 33 MHz |
| Apex EP20K60E-1 | 1649 | 3 ESB | 384 | 40 MHz |
| Cyclone EP1C20-6 | 1584 | 3 M4K | 384 | 78 MHz |
| Stratix EP1S20-5 | 1584 | 3 M512 | 384 | 80 MHz |
| Stratix-II EP2S60-3 | 1379 | 3 M512 | 384 | 117 MHz |

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The CAN controller has been implemented into Fraunhofer-IPM 1.0 micron double metal CMOS technology library and has been tested successfully. The megafunction has also been certified by a Bosch reference model.

Deliverables

The megafunction includes everything required for successful implementation:

Netlist License

- Post-synthesis EDIF netlist
- Assignment & Configuration
- Symbol & Include files
- Testbench (self checking)
- Vectors & expected results for testing functionality
- Documentation

HDL Source License

- VHDL or Verilog RTL source code
- Testbenches (self checking)
- Wrapper for pin compatible replacement
- Vectors & expected results for testing functionality
- Synthesis and simulation scripts
- Documentation