**CAN-CTRL**

**CAN 2.0 & CAN FD Bus Controller Core**

Implements a CAN protocol bus controller that performs serial communication according to the CAN 2.0A, 2.0B, and the Bosch CAN FD Flexible Data-Rate specifications.

The CAN protocol uses a multi-master bus configuration for the transfer of frames between nodes of the network and manages error handling with no burden on the host processor. The core enables the user to set up economic and reliable links between various components. It appears as a memory-mapped I/O device to the host processor, which accesses the CAN core to control the transmission or reception of frames.

The CAN core is easy to use and integrate featuring programmable interrupts, data and baud rates; a configurable number of independently programmable acceptance filters; and a generic processor interface or optionally an AMBA APB, or AHB-Lite interface. It implements a flexible buffering scheme, allowing fine-tuning of the core size to the requirements of each specific application. The number of receive buffers is synthesis-time configurable. Two types of transmit buffers are implemented: a high-priority primary transmit buffer (PTB) and a lower-priority secondary transmit buffer (STB). The PTB can store one message, while the number of included buffer slots for the STB is synthesis-time configurable 0 to 16 slots. Moreover, an optional wrapper instantiating multiple CAN controller cores eases integration in cases where multiple bus-nodes need to be controlled by the same host processor.

The core implements functionality similar to the Philips SJA1000 working with its PeliCAN mode extensions, providing error analysis, diagnosis, system maintenance and optimization features.

Additionally, the core offers a CAN FD extension to increase net data throughput. It comprises data fields up to 64 bytes, extended CRC checksum, and a higher data rate for the data phase.

The CAN core is robustly verified and proven in multiple production designs.

**Applications**

The CAN-CTRL core can be integrated in devices that use CAN or higher-layer, CAN-based communication protocols. In addition to traditional automotive applications, such devices are used in industrial (e.g. the CANopen and DeviceNet protocols), aviation (e.g. the ARINC-825 and CANaerospace protocols), marine (e.g. the NMEA 2000 protocol) and other applications.

**Block Diagram**
**Functional Description**

The CAN bus core is founded on the basic CAN principle and meets all constraints of the CAN-specification 2.0B. Several 13-byte buffers are used for buffering received or transmitted messages. The number of buffers can be selected before synthesis. Selecting a large number of buffers disables the need for real-time reaction to CAN messages for the host processor, which significantly eases software development of the system application.

The included high-priority transmit buffer can be used to transmit an important message as fast as possible, even if several lower-priority messages are pending for transmission.

The host interface contains all necessary registers for controlling and configuring the core. The host is able to read and write all registers as a conventional RAM in memory mapped mode.

The interface to the host is software configurable. All events on the CAN data bus or in the CAN controller core are signaled using an interrupt. Every interrupt source may be individually enabled or disabled. The CAN controller core contains up to sixteen software-programmable 29-bit acceptance filters that can be used to block unwanted CAN messages, which reduces the load to the host controller.

The host controller interface is connected with the memory module by an 8-bit data and an 8-bit address bus. This enables easy interfacing to many host controller types, and therefore, quick integration with a microcontroller.

**Support**

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

**Verification**

The core has been rigorously verified and has been production proven multiple times.

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**Implementation Results**

CAN reference designs have been evaluated in a variety of technologies. The following are sample results optimized for area with 3 receive buffers, 3 transmit buffers and 3 acceptance filters and without the CAN FD option.

<table>
<thead>
<tr>
<th>Family</th>
<th>Utilization (Cells or Tiles)</th>
<th>Freq. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Sequential</td>
<td>Combinatorial</td>
</tr>
<tr>
<td>ProASIC3PLUS A3PA1000-2</td>
<td>548</td>
<td>3335</td>
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<tr>
<td>Áxcelerator AX1000-2</td>
<td>636</td>
<td>2088</td>
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<tr>
<td>IGLOO AGL1000V5-std</td>
<td>547</td>
<td>3339</td>
</tr>
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**Deliverables**

The core includes everything required for successful implementation:

- VHDL or Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbenches
  - Behavioral tests
  - Post-synthesis verification
- Simulation scripts
- Synthesis scripts
- Documentation