CAN-CTRL
CAN 2.0 & CAN FD Bus Controller Core

Implements a CAN bus controller that performs serial communication according to CAN 2.0, and CAN FD specifications. It supports the original Bosch protocol and ISO specifications as defined in ISO 1989—including time-triggered operation (TTCAN) as specified in ISO 19898-4—and is also optimized to support the popular AUTOSAR and SAE J1939 specifications.

The CAN protocol uses a multi-master bus configuration for the transfer of frames between nodes of the network and manages error handling with no burden on the host processor. The core enables the user to set up economic and reliable links between various components. It appears as a memory-mapped I/O device to the host processor, which accesses the CAN core to control the transmission or reception of frames.

The CAN core is easy to use and integrate, featuring programmable interrupts, data and baud rates; a configurable number of independently programmable acceptance filters; and a generic processor interface or optionally an AMBA APB, or AHB-Lite interface. It implements a flexible buffering scheme, allowing fine-tuning of the core size to satisfy the requirements of each specific application.

The number of receive buffers is synthesis-time configurable. Two types of transmit buffers are implemented: a high-priority primary transmit buffer (PTB) and a lower-priority secondary transmit buffer (STB). The PTB can store one message, while the number of included buffer slots for the STB is synthesis-time configurable. The transmit buffer can operate in FIFO or priority mode.

The core implements functionality similar to the Philips SJA1000 working with its PeliCAN mode extensions, providing error analysis, diagnosis, system maintenance, and optimization features.

The CAN-CTRL is available in two versions: Normal, and Safety-Enhanced. The Safety-Enhanced version implements ECC for SRAMs protection and uses spatial redundancy for protecting the inner logic of the core. The deliverables for this version include a Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA), and the /ISO-26262 ASIL-B Ready certificate, issued by SGS-TÜV Saar GmbH. An ASIL-C compatible version can be made available and get certified up on request.

The core is extensively verified, proven in several plug fests and a large number of production designs.

Block Diagram
Applications

The CAN-CTRL core can be integrated in devices that use CAN or CAN-based communication protocols. In addition to traditional automotive applications, such devices are used in industrial (e.g. the CANopen and DeviceNet protocols), aviation (e.g. the ARINC-825 and CAN aerospace protocols), marine (e.g. the NMEA 2000 protocol) and other applications.

Functional Description

The CAN bus core is founded on the basic CAN protocol principle and meets all constraints of the CAN 2.0B and CAN FD specifications.

Several message buffers are used for buffering received or transmitted messages. The number of buffers can be selected before synthesis. Selecting a large number of buffers disables the need for real-time reaction to CAN messages for the host processor, which significantly eases software development of the system application.

The included high-priority primary transmit buffer (PTB) can be used to transmit an important message as fast as possible, even if several lower-priority messages are pending. The secondary transmit buffer (STB) operates either in FIFO mode or in priority mode where the order is changed depending on the message priority.

The host interface contains all necessary registers for controlling and configuring the core. The host is able to read and write all registers as conventional RAM in memory mapped mode.

The interface to the host is software configurable. All events on the CAN data bus or in the CAN controller core are signaled using an interrupt. Every interrupt source may be individually enabled or disabled. The CAN controller core contains up to sixteen software-programmable 29-bit acceptance filters that can be used to block unwanted CAN messages, which reduces the load to the host controller.

The host controller interface operates in a different clock domain, which can be synchronous or asynchronous to the core clock. The host-interface type is 32-bit and can be customized with available wrappers to either an 8-bit-wide generic processor interface or a 32-bit-wide APB or AHB-lite interface. This enables easy interfacing to many host controller types, facilitating quick integration with a microcontroller. Furthermore, the width of the internal data path and buffers is adjusted depending on the host interface to ensure efficient utilization of the host bus bandwidth.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

The CAN-CTRL can be mapped to any Intel FPGA device (provided sufficient silicon resources are available). The following are sample results for the core configured with three receive buffers, three transmit buffers, and three acceptance filters (does not include priority mode, TTCAN and CiA603 timestamping). Please contact CAST to get characterization data for your target configuration and technology.

<table>
<thead>
<tr>
<th>Family Device</th>
<th>CAN 2.0</th>
<th>CAN-FD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Logic</td>
<td>Memory</td>
</tr>
<tr>
<td>Max 10M50</td>
<td>2,343 LEs</td>
<td>0 MULTs</td>
</tr>
<tr>
<td>Cyclone V</td>
<td>1,094 ALMs</td>
<td>1 DSP</td>
</tr>
<tr>
<td>SCEFA7</td>
<td></td>
<td>1,088 bits</td>
</tr>
<tr>
<td>Cyclone 10 LP</td>
<td>1,331 ALMs</td>
<td>0 MULTs</td>
</tr>
<tr>
<td>10CL120</td>
<td>3 RAM Blocks</td>
<td></td>
</tr>
<tr>
<td>Cyclone 10 GX</td>
<td>1,072 ALMs</td>
<td>1 DSP</td>
</tr>
<tr>
<td>10AX115</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Arria 10 GX</td>
<td>1,117 ALMs</td>
<td>1 DSP</td>
</tr>
<tr>
<td>10AX115</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Host and CAN clock constrained to 80MHz

Verification

The core has been rigorously verified and has been production proven multiple times.

The core has been verified through extensive synthesis, place and route, simulation runs, Verification IP, and PlugFests. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including:

- VHDL or Verilog RTL source code
- Post-synthesis netlist (netlist licenses)
- Testbenches
  - Behavioral tests
  - Post-synthesis verification
- Simulation scripts
- Synthesis scripts
- Linux driver
- Documentation

The optional safety-enhanced package includes the Safety Manual (SAM), a Failure Modes, Effects and Diagnostics
Analysis (FMEDA) and the ASIL-B Ready certificate, issued by SGS-TÜV Saar GmbH.