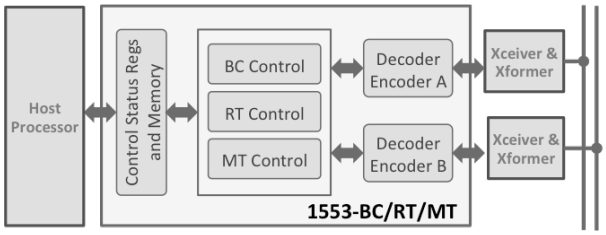
1553-BC/RT/MT

MIL-STD-1553 Bus Controller, Remote & Monitor Terminal Core

The 1553-BC/RT/MT IP core implements a serial link controller enabling the development of Bus Controllers (BC), Remote Terminals (RT), and Monitor Terminals (MT) compliant with the Department of Defense MIL-STD-1553B standard. Field-proven in many civilian and military avionics systems and optionally accompanied by a DO-254 certification package, the core is highly reliable and ready for aviation applications.

The core can operate as a Bus Controller, Remote Terminal, and Monitor Terminal at the same time. The BC and RT modules can also be disabled at run time, or at synthesis time to reduce silicon requirements. The Monitor Terminal provides 1553 Bus Monitor (BM) functions within the core. It is available under all configurations, and can be enabled or disabled at run time.



The 1553-BC/RT/MT is designed to enable flexible message scheduling, monitoring, and filtering for all types of traffic in different bus architectures and with minimum overhead for the host processor. Messages are conveyed to/from the host via shared memory space organized in 16-bit words, and configure the core via its 16-bit wide register interface. Once the host sets up one or more transmissions, the core operates on standalone basis, and the host is only required to respond on transmission events (e.g. reception of all data or error detection).

Compatibility with popular IC devices enables the core to work with industry-standard drivers and software applications. Special versions are available for drop-in replacement of legacy ICs.

The 1553-BC/RT/MT core is designed with industry best practices, and its reliability has been proven in real-life in many civilian and military avionics systems. The core is available in VHDL RTL or as targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation. An FMC FPGA board is also available for evaluating or in-field testing the core.

Applications

The 1553-BC/RT/MT is suitable for the implementation of MIL-STD-1553B Bus Controllers (BC), Remote Terminals (RT), and Bus Monitors (BM) in avionics systems.

Features

DO-254 certifiable, highly-featured MIL-STD-1553B link controller

MIL-STD-1553 Link Controller

- BC/RT/MT; BC-only, RT-only and Multi-RT configurations
- Supports dual-redundant buses
- Supports flexible message scheduling and minimizes host processor load
  - Programmable auto-repeat retry-on-error, and stop-on-error modes
  - Programmable inter-message gap (4µs to 65.5ms)
- Enables efficient message monitoring and filtering for all types of traffic
  - Up to 30 Rx and 30 Tx programmable sub-addresses
  - Single, Dual, and Circular data buffering modes
- Error detection and status reporting for all transactions

Reliable and Proven

- Deployed in many military and civilian avionic systems
- Verified with numerous transceiver-transformer pairs.
- Optionally delivered with DO-254 Certification Data Package
- FMC FPGA board available for evaluation and/or in-field testing

Easy to Use

- Compatible with industry-standard devices, enables use of existing software drivers and applications
- Special versions available for replacement of legacy ICs

Deliverables

- Source-code VHDL RTL or targeted netlist
- Test-bench
- Comprehensive documentation
- Optional DO-254 package for all certification levels.

Silicon Resources Requirements

The core can be mapped to any ASIC technology and FPGA devices from Intel/Altera, Lattice, Microsemi, or Xilinx, and its silicon resources requirements depend on its configuration. The following table provides indicative implementation results.

Configuration	Target Technology	Area
BC-Only	Altera, Arria10	5,400 ALMs, 2 DSPs, 2 M20K
	Xilinx, Kintex7	6,900 LUTs, 3 DSPs, 0 BRAM
RT-Only	Altera, Arria10	2,950 ALMs, 0 DSP, 1 M20K
	Xilinx, Kintex7	2,900 LUTs, 0 DSPS, 1 BRAM

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