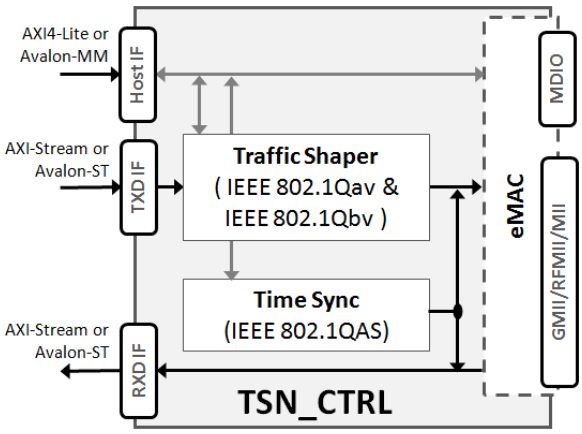
TSN_CTRL

TSN Ethernet Subsystem

The TSN_CTRL implements a configurable subsystem meant to ease the implementation of endpoints for networks complying to the Time Sensitive Networking (TSN) standards. It integrates hardware stacks for timing synchronization (IEEE 802.1AS) and traffic shaping (IEEE 802.1Qav and 802.1Qbv), and a low-latency Ethernet MAC.

The subsystem is designed to enable high-precision timing synchronization and flexible yet accurate TSN traffic scheduling. Requiring no software assistance for its operation, it features minimal and deterministic ingress and egress latencies, and simplifies the development of time-aware applications.



While operating autonomously, the TSN_CTRL provides the system with timing information (time-stamps, alarms, etc.) that is typically required for the operation of a TSN network bridge or node. Furthermore, it allows the system to define and tune in real time the traffic shaping parameters according to an application's requirements.

The TSN_CTRL uses standard AMBA® or Avalon® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit-wide AXI4-Lite or Avalon-MM bus, and packet data are input and output via AXI-Streaming or Avalon ST interfaces with 8-bit data buses.

The TSN_CTRL subsystem is designed with industry best practices, and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications

The TSN_CTRL is suitable for the implementation of sources of traffic and bridges for TSN Ethernet networks requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, and aerospace applications.

Options

The TSN_CTRL can be modified to meet the requirements of different applications in the following ways:

- Use of a 3rd party Ethernet MAC IP core. Versions integrating the Ethernet MAC core from Intel and Xilinx are readily available.
- The Timing Synchronization, Traffic Shaping, and Ethernet MAC modules can be made independently available as standalone IP cores.
- The TSN_CTRL can be integrated with a hardware UDP/IP stack.

Features

Subsystem suitable for the implementation of bridges or nodes for automotive or industrial Ethernet; integrates three IP cores:

IEEE 802.1AS Hardware Stack

- Autonomously synchronizes internal Real-Time Clock to Grandmaster's time
- Returns timestamps to the system using absolute time
- Provides periodic event triggers and alarm to assert host interrupt at specified absolute time
- Automatically calculates point-to-point latency
- Supports optional timer precision improvement by the host
- Supports full-duplex, point-to-point links
- Supports time-aware end-points – not Grandmaster capable

IEEE 802.1Qav and 802.1Qbv Hardware Stack

- Supports up to 8 traffic classes, as per VLAN (IEEE 802.1Q)
- Enables bandwidth reservation and allocation per traffic class, and deterministic, low-latency, low-jitter communication for all traffic classes (IEEE 802.1Qav and IEEE 802.1Qbv)

Low-Latency Ethernet MAC

- Enables high-precision synchronization in TSN networks
  - Egress latency: 10 Tx clock cycles
  - Ingress latency: 6 Rx clock cycles
- 10/100/1000 Mbit/s Ethernet and MII, GMII and RGMIII PHY interfaces

Easy System Integration

- Autonomous operation, requires no host assistance once programmed
- AMBA/AXI4 or Avalon Interfaces
  - AX4-Lite host interfaces, and AXI4-Stream for packet data
  - Avalon-MM host interface and Avalon-St for packet-data
- Complete reference designs available for Altera and Xilinx, including sample application software

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Support

The subsystem as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The subsystem has been rigorously verified, hardware-validated and tested in real-life environments.

Deliverables

The subsystem includes everything required for successful implementation:

- Verilog RTL source code or targeted PFGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation

Related Products

The core is a member of CAST's family of automotive interface products that includes:

- CAN 2.0/CAN-FD Controller IP core
- CAN 2.0/CAN-FD Verification IP
- CAN-2.0/CAN-FD Transceiver daughter card
- CAN-FD FPGA Reference design
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core

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Fraunhofer IPMS

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