IEEE802_1AS

IEEE 802.1AS Hardware Protocol Stack

The IEEE802_1AS is a complete IEEE 802.1AS hardware stack that enables the simple and rapid development of time-aware nodes for AVB/TSN networks such as automotive Ethernet. It operates fully autonomously and provides timing and synchronization according to IEEE 802.1AS for full-duplex, point-to-point Ethernet links.

The core is designed to operate next to an Ethernet Media Access Control unit (eMAC) and attached to that eMAC's data-interface towards the host system. It automatically synchronizes its internal real-time clock (RTC) to that of the grandmaster by inserting and extracting IEEE 802.1AS frames in and from the Ethernet traffic. The core fully offloads the host processor from any IEEE 802.1AS related processing, and at the same time enables the development of time-aware applications: it provides timestamps, periodic event triggers, and alarms to the host system, using host processor Interrupt lines or dedicated-low latency interface signals.

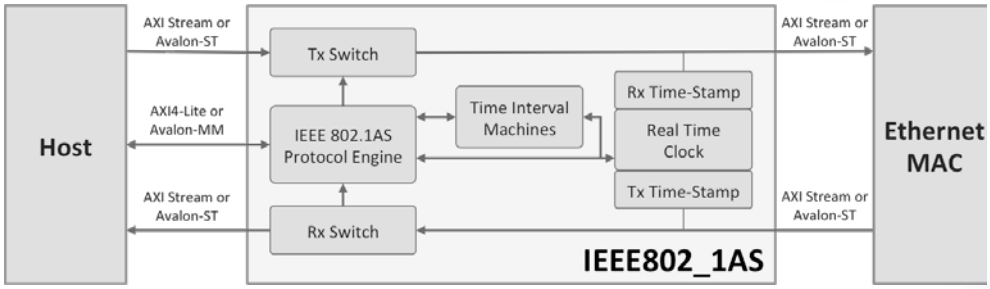
The core uses standard AMBA® or Avalon® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit wide AXI4-Lite or Avalon-MM bus, and Ethernet frame packet data are input and output via AXI-Streaming or Avalon ST interfaces with 8-bit data buses. Furthermore, the core causes no constraints with respect to system clocking, as it assumes separate and independent clocks for each of its interfaces (i.e., host, tx data, and rx data), and separate and independent clocks for its RTC and internal timers. To further ease integration, the core is available pre-integrated with either Intel/Altera's eMAC cores. Integration with other 3rd party eMAC cores is also possible using CAST"s design integration services. Complete reference designs on commercially available FPGA boards are also available, and can be used for on-field testing or as templates to speed-up application development.

The IEEE802_1AS core is designed with industry best practices. The design is CDC-clean, LINT-clean, and scan-ready. The core is available in synthesizable RTL (Verilog 2001) source code or as targeted FPGA netlists. Deliverables provide everything required for a successful implementation, including sample scripts, a testbench, and comprehensive documentation.

Applications

The IEEE802_1AS protocol stack is suitable for implementing time-aware network nodes for applications requiring very low transmission latency and high availability, such as audio/video streaming and real-time control in automotive or industrial environments.

Block Diagram



Features

Complete IEEE 802.1AS hardware stack enabling rapid development of time-aware AVB/TSN nodes

IEEE 802.1AS Hardware Stack

- Supports full-duplex, point-to-point links
- Automatically synchronizes internal Real-Time Clock to Grandmaster's time
  - Automatically calculates point-to-point latency
  - Has programmable eMAC and PHY ingress and egress latency
  - Allows high timer frequency to minimize quantization error
  - Supports RTC precision fine-tuning by the host (optional)
  - Real time clock in seconds (48 bit), nanoseconds (32 bit) and fractional nanoseconds (16 bit)
- Supports time-aware end points – Not Grandmaster capable

Enables Time-Aware Application Development

- Returns timestamps to the system using absolute time
  - Timestamp requested via software or lower latency hardware interface
  - Timestamps have 802.1AS accuracy (seconds and nanoseconds)
- Programmable alarm to assert host interrupt at specified absolute time
- Provides periodic event triggers
  - Events periods are independent from absolute time changes
  - Each event triggers a maskable host interrupt and/or toggles a dedicated hardware line, which the system can use as a clock

Eases Integration

- AMBA/AXI4 or Avalon Interfaces
  - AX4-Lite host interfaces, and AXI4-Stream for packet data
  - Avalon-MM host interface and Avalon-St for packet-data
- Independent clocks for internal timers and for each of the interfaces (rx data, tx data, host)
- Clean clock-domain-crossing, LINT-clean and scan-ready design
- Pre-integrated with Intel/Altera Ethernet MAC cores; services available for integrating with other 3rd part eMAC cores
- Complete reference designs for Intel/Altera, including sample application software

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Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been rigorously verified, hardware-validated and tested in real-life environments.

Implementation Results

IEEE802_1AS core reference designs have been evaluated in a variety of technologies. The following table provides Intel/Altera indicative implementation results, when all core clocks are constrained to 125 MHz, which is sufficient for a 1Gbps throughput on each direction. These sample results do not represent minimum area for the core. Mapping to other Intel/Altera devices is possible.

Technology	Area	Freq (MHz)
Altera – Arria10	3,900 ALMs	125

Deliverables

The core includes everything required for successful implementation:

- Targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation

The Intel/Altera release also includes a QSYS project using a NIOS-based microcontroller system, and an Altera Eclipse project for a sample software application.

Related Products

The core is a member of CAST's Automotive Interfaces IP family, which includes:

- CAN 2.0/CAN-FD Controller IP core
- CAN 2.0/CAN-FD Verification IP
- CAN-2.0/CAN-FD Transceiver daughter card
- CAN-FD FPGA Reference design
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core

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This core is sourced from
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