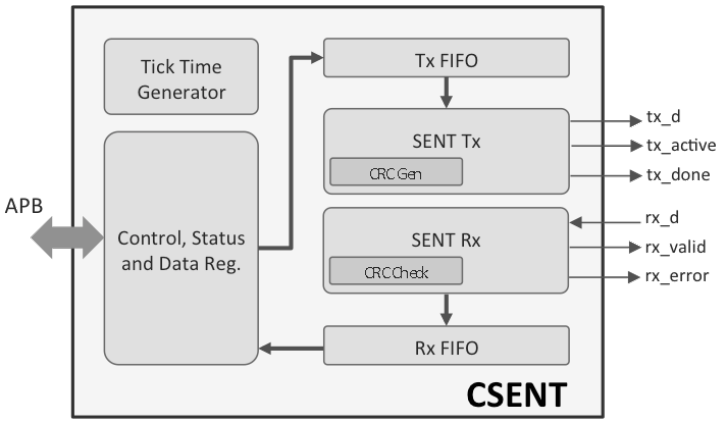
CSENT

SENT / SAE J2716 Controller Core

The CSENT core implements a controller for the Single Edge Nibble Transmission (SENT) protocol. It complies with the SAE J2716 standard and also the industry de-facto standard Short PWM Code (SPC) protocol, and can be used for conveying data from one or multiple sensors to a centralized controller using a single SENT line.



The CSENT core can be configured as a Transmitter and/or as a Receiver, and therefore it is suitable for adding a SENT interface to devices transmitting sensor data or to controllers receiving sensor data. It provides access to its control, status, and data registers via a 32-bit APB bus interface, and a comprehensive set of interrupt signals facilitates interrupt-based operation. The core allows for Transmitter operation without requiring any external programming or control. The reset values for all its control registers are defined at synthesis time, and at run time the system only needs to write sensor data to the core.

The CSENT core is designed with industry best practices. The core contains no latches or tri-sates, and is fully synchronous with a single clock domain. The core is available in Verilog RTL or as targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications

The CSENT core is suitable for designing low-cost digital automotive sensors, and automotive controller units.

Size and Performance

The core can be mapped to any ASIC technology and any FPGA device from Intel/Altera, Lattice, Microsemi, or Xilinx. The following are sample implementation results, which do not represent the highest speed or smallest area possible for the core and do not include the area for the implementation of the FIFOs.

Configuration	Target Technology	Area	Fmax
Tx and Rx	TSMC 28hpm	2410 um^2 / 4,850 Gates	1000 MHz
	Xilinx, Kintex-7	781 LUTs	361 MHz
	Altera, Stratix V	570 ALMs	315 MHz
Tx only	TSMC 28hpm	1152 um^2 / 2,300 Gates	1000 MHz
	Xilinx, Kintex-7	430 LUTs	358 MHz
	Altera, Stratix V	275 ALMs	339 MHz

Features

SENT / SAE J2716 Receiver & Transmitter

- Fast and Slow Channel Transmit or Receive
- CRC generation for Transmitter, and CRC checking for Receiver
- All types of SENT Frames
  - Programmable data length (4 to 24 bits) for Fast Channel Frames
  - Short (8-bit data) and Enhanced (12- or 16-bit data) Message Formats for Slow Channel
- Optional Pause Pulse with programmable length
- Supports inverted SENT protocol

Short PWM Code (SPC) Receiver & Transmitter

- Allows up to four sensors (transmitters) to use the same physical SENT connection
- Programmable master trigger pulse length

Ease of Integration

- 32-bit APB interface, and comprehensive set of interrupts
- Programmable 4-bit clock divider and high precision 16-bit clock pre-scale
- Receive and Transmit FIFO of configurable size for Fast Channel data
- Run-time programmable configuration registers
- Synthesis-time defined reset values for all registers, enables data transmit without control from host processor
- LINT-clean, single-clock domain, scan-ready design

Deliverables

- Source code Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Documentation

CAST, Inc. 50 Tice Blvd, Suite 340, Woodcliff Lake, NJ 07677 USA, tel 201-391-8300 fax 201-391-8694