CAN2TSN

CAN-to-TSN Ethernet Gateway/Bridge

The CAN2TSN IP subsystem implements a CAN-to-TSN Ethernet gateway. It enables low-latency, bidirectional communication between up to seven CAN bus ports and one Time-Sensitive Networking Ethernet port.

The CAN ports can be connected to the same or different CAN networks, and each is independently programmable with the payload type (CAN 2.0 or CAN FD) and data rate. The Ethernet port is connected to a 10/100/1000 Mbit network, and supports gPTP/IEEE 802.1AS timing synchronization and traffic shaping according to the IEEE 802.1Qav and IEEE 802.1Qbv standards.

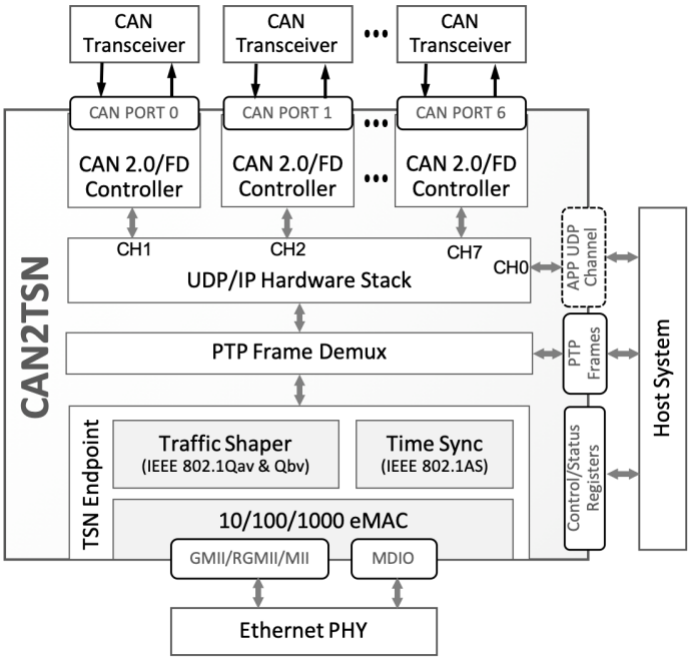
The CAN2TSN timestamps received CAN messages, encapsulates them to UDP frames, and transmits them over Ethernet. In the opposite direction, the CAN2TSN accepts UDP frames encapsulating CAN messages, and extracts and forwards each to one of the CAN ports for transmission.

Each CAN port is associated with a UDP destination port and represents a traffic class for traffic shaping purposes on the Ethernet side. The latency in both directions, CAN to Ethernet and Ethernet to CAN, is extremely low (<30µs), making the gateway suitable for real-time control applications.

To simplify system integration, the CAN2TSN uses standard interfaces and requires minimal software assistance. It interfaces with the SoC via AMBA™ AXI4 buses. It connects to the Ethernet PHY via a standard MII, GMII, or RGMII interface, and to the external CAN transceivers via an industry-standard three-wire (Rx, Tx, STBY) interface. The gateway implements DHCP, ARP, ICMP, UDPIP, IEEE 802.1Qav, and IEEE 802.1Qbv with custom hardware; only part of the gPTP stack is implemented in software to allow easy adaptation to future versions of the timing synchronization protocol. The lightweight gPTP software stack runs under FreeRTOS, and can be easily ported to another real-time operating system.

The CAN2TSN is designed with industry best practices, and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, testbench, and comprehensive documentation.

Block Diagram



FEATURES

CAN-to-TSN Gateway

- Enables bidirectional communication between up to seven CAN ports and one Ethernet port
- UDP Encapsulation of CAN messages
  - CAN2.0 and CAN FD messages
  - Timestamps per CAN message
  - UDP port number selects the CAN Bus node
  - Multiple CAN messages in one UDP frame for better utilization of Ethernet bandwidth
- Less than 30µs latency

CAN Features

- Programmable payload type (CAN 2.0 or CAN FD) and data rate per CAN node
- Up to 16 programmable 29-bit acceptance filters per CAN node
- Configurable number of receive buffers
- One high-priority transmit buffer
- Configurable number of lower-priority transmit buffers

Ethernet Features

- IPv4 support without packet fragmentation
- ARP support with IP Cache
- ICMP support (Ping Reply)
- UDP Support
- UDP Port Filtering
- UDP/IP Unicast, Multicast and Broadcast
- DHCP support

TSN Ethernet Features

- Time Synchronization
  - Supports gPTP/IEEE 802.1AS. Filters out PTP frames and forwards them to the system for further processing
  - RTC & hardware timestamps for transmission and reception
- Traffic Shaping
  - Implements IEEE 802.1Qav (credit-based shaper) & IEEE 802.1Qbv (time aware scheduling)
  - Configurable up to 256 control list entries
  - 2-8 traffic classes (configurable)

Easy System Integration

- Configuration & status registers accessible via an AXI4-Lite slave port
- Sample gPTP stack over FreeRTOS
- Complete FPGA reference designs available.

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Applications

The CAN2TSN can be used in industrial control or automotive systems, where devices with CAN bus connectivity coexist with devices with TSN Ethernet connectivity.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The CAN2TSN has been rigorously verified, hardware-validated, and tested in real-life environments.

The subsystem was developed by integrating proven IP cores from CAST: the CAN controller, and the UDPIP hardware stack IP cores are hundreds of times production proven, and the TSN Ethernet Endpoint has been Interoperability tested and verified at TSN plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted PFGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation

Related Products

The core is a member of CAST's family of automotive interface products that includes:

- CAN 2.0/CAN FD Controller IP core
- TSN-EP TSN Ethernet Endpoint IP core
- TSN-SE TSN Ethernet Switched Endpoint IP core
- UDPIP-1G/10G UDP/IP Hardware Protocol Stack IP core
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- SENT and LIN protocol controller IP cores