

CAST



SVE-JPEG-E

SpeedView Enabled JPEG Encoder Core

The SVE-JPEG-E core implements a high-performance image encoder that produces SpeedView™ enabled JPEG data streams.

Integrating the SpeedTags™ technology the SVE-JPEG-E outputs compressed streams that are compatible with SpeedView™, a member of Scalado's CAPS™ imaging suite which is focused on providing enhanced functionality to camera equipped mobile devices. CAPS™ compatibility combined with a hardware architecture being able to process more than 500MSamples/sec, makes the SVE-JPEG-E a unique solution for multi-megapixel applications.

Furthermore, the SVE-JPEG-E can be configured to output streams compatible to baseline JPEG, or non-standard motion-JPEG streams. Finally the core can be enhanced with a bit-rate control block, which may benefit applications that have tight bandwidth constraints.

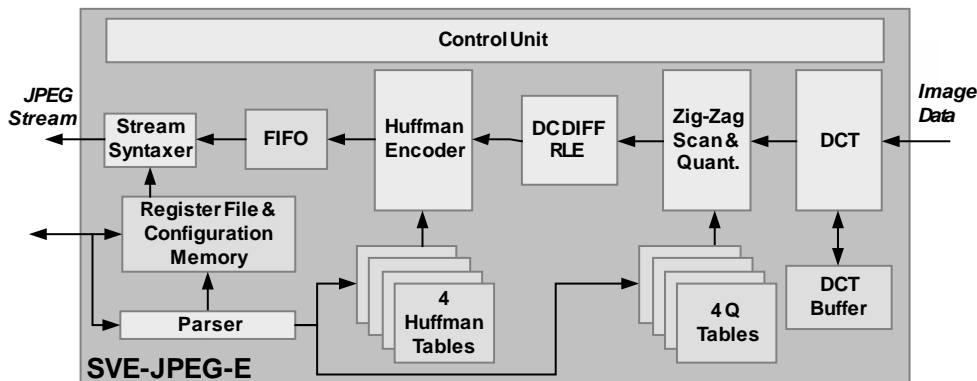
Designed for ease of integration the core includes FIFO-like pixel and stream input/output interfaces. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance SVE-JPEG-E core is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems
- Camera equipped mobile devices, such as PDAs, and Camera phones

Block Diagram



Features

Scalado CAPSTM Compliance

- Integrates SpeedTags™ technology

JPEG Features

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Additional Image Processing Capabilities

- Motion JPEG encoding/decoding
- Rate-Control (optional)

Designed for Easy Integration

- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- Scan-ready design architecture

Functional Description

The SVE-JPEG-E core is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the SVE-JPEG-E in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the SVE-JPEG-E can address the most demanding frame-based video compression applications. The SVE-JPEG-E outputs a complete JPEG data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used. Output JPEG stream can be either compatible to JPEG standard or to CAPS™ imaging suite.

Support

SVE-JPEG-E reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with all core I/Os assumed to be routed on-chip.

Xilinx Device	Slices	BRAM	Special Features	I/Os	Fmax (MHz)	ISE
Spartan-3E 3S500E-5	2,750	7	10 MULT	80	110	10.1i
Virtex-4 4VLX15-12	2,370	7	9 DSP	80	170	10.1i

Support

The SVE-JPEG-E core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The SVE-JPEG-E core has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA technologies.

Deliverables

The SVE-JPEG-E is available as a soft core (synthesizable HDL) for ASIC technologies and as a firm core (netlist) for FPGA technologies, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Place and route script
- Simulation script, vectors and expected results
- Sophisticated HDL Testbench
- Software (C++) Bit-Accurate Model
- Comprehensive user documentation, including detailed specifications and a system integration guide