

# CAST

## LJPEG-E

### Lossless JPEG Encoder Core

The LJPEG-E core implements the Lossless JPEG (LJPEG) compression in a compact, high-performance, stand-alone package ideal for applications where bit-by-bit accurate reproduction of an image is essential.

The LJPEG-E conforms to the spatial (sequential) lossless encoding mode (SOF3) of the ISO/IEC 10918-1 standard (CCITT T81 recommendation). Rather than the Discrete Cosine Transform (DCT) functions used for lossy JPEG compression - which can introduce round-off errors - the LJPEG-E employs a predictor function as described in the specification. It thus encodes and compresses images with no information loss, and requires a significantly smaller physical implementation.

Evaluation designs show that the core requires just 21K gates in an ASIC. Its heavily optimized architecture also enables very high performance, reaching 500 MSamples/sec on 0.09 $\mu$  process (under typical process and operating conditions).

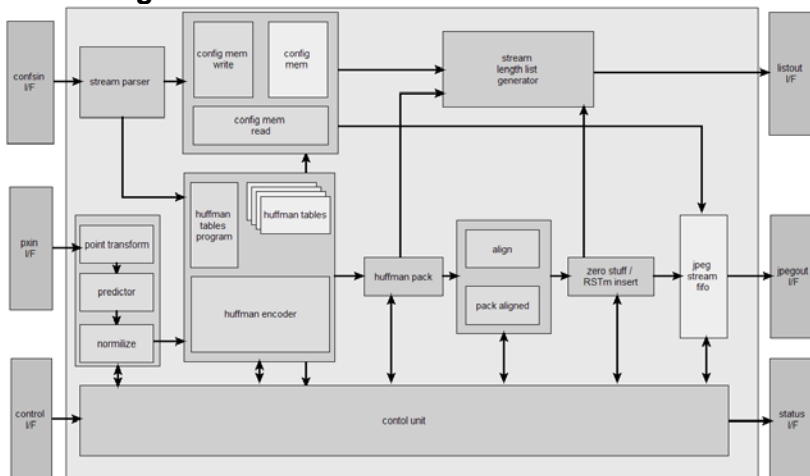
The LJPEG-E is a fully synchronous, strictly positive-edge design with no internal three-state buffers. Comprehensive documentation and a complete verification environment - including a bit-accurate model - help designers integrate and verify the core.

## Applications

The LJPEG-E provides a fast, economical solution whenever lossless image compression is essential, including applications such as:

- Medical, military, and space imaging.
- Professional, studio-quality cameras and editing suites.
- High-end film and photo scanners.
- Industrial machine vision systems.

## Block Diagram



## Features

- Conforms to the spatial (sequential) lossless encoding mode (SOF3) of the ISO/IEC 10918-1 standard (CCITT T.81 recommendation).
- Standalone operation.
  - Pixel samples input.
  - Standalone ISO/IEC 10918-1 JPEG stream output.
- Easily programmable through standard JPEG markers stream.
  - Programmable image dimensions.
  - Full range sample precision support (2 to 16 bits per sample)
  - Up to four stream programmable Huffman tables.
  - Programmable Restart Interval.
  - Programmable Point Transform function.
  - Programmable APPn and COM markers.
  - Programming errors catch-up features.
- Compact, high-performance architecture.
  - 21K gates achieving 500 MSamples/sec (0.09 $\mu$  ASIC) under typical process and operating conditions.
  - Also fits inexpensive FPGAs (see FPGA version data-sheets)
- Robust and simple to use
  - General purpose, fully stallable, streaming I/O interfaces.

## Limitations with respect to the ISO/IEC 10918-1 standard:

- Up to three image-components are supported (Nf field of the SOF3 marker segment = 1 or 2 or 3).
- Single scan encoding (only one SOS marker segment, with Ns field = Nf).
- No DNL marker insertion (Y field of the SOF3 marker segment > 0).
- Fixed parameters.
  - No sub-sampling (Hi and Vi fields of the SOF3 marker segment = 1).
  - Prediction function is fixed to the left-hand predictor, predictor 1. (Ss field of SOS marker segment = 1).

## Functional Description

Lossless JPEG was added to the ITU-T JPEG recommendations in 1995. The JPEG lossless mode of operation does not use the 2D-DCT that is used in the lossy mode, since round-off errors prevent a 2D-DCT calculation from being lossless. For the same reason, one would not normally use color space conversion or down-sampling, although these are permitted by the standard.

The lossless mode of the standard codes the difference between each pixel and the "predicted" value for the pixel. The predicted value is a function of the already-transmitted pixels just above and to the left of the current one (eight different predictor functions are defined in the standard). The sequence of the calculated differences (prediction errors) is encoded using the same back end (Huffman or arithmetic) used in the lossy mode. The LJPEG-E core implements the predictor 1 function of the standard, and the Huffman coding back end.

The LJPEG-E core is initially configured using standard JPEG marker segments from the configuration stream input interface. It is configured for frame properties using a standard SOF3 marker segment. Huffman tables that will be used for encoding are programmed through one or more DHT segments. If the restart interval and/or point transform functions are required, they are programmed through the standard DRI and SOS marker segments respectively. If the application needs to use comment and/or application markers, then these are programmed using COM and/or APPn segments and the LJPEG-E will include them in the output stream.

Following initial configuration, the LJPEG-E is ready to accept and encode image frames. Pixel data are written to the core through the pixel input interface and the compressed data are output through the JPEG stream output interface. Configuration can remain constant between consecutive frames or it can change to meet specific frame requirements. In the compressed output stream, the LJPEG-E includes all the necessary markers so that the produced stream is a full, standalone JPEG stream that can be decoded by any ISO/IEC 10918-1 compliant lossless JPEG decoder.

## Implementation Results

LJPEG-E core has been evaluated in a variety of technologies. The following are sample pre-layout ASIC results (as reported by the synthesis tool and silicon vendor design kit) under typical process and operating conditions, with all core I/Os assumed to be routed on-chip, logical area excluding memory, and with equivalent gates count calculation using the smallest NAND2 gate available in the technology.

ASIC Technology	Fmax (MHz)	Logic Area (um <sup>2</sup> )	Number of eq. gates	Memory (bits)
TSMC 0.18μ process	300	~244K	25K	6,912
TSMC 0.09μ process	500	~59K	21K	6,912

## Support

The LJPEG-E core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The LJPEG-E core has been verified through extensive simulation using a large set of test vectors and reference results, and through rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- A bit-accurate model (BAM) including custom vector generation support, and a software library of the bit accurate model functions.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including test vectors, expected results, and verification engine.
- Simulation scripts.
- Synthesis script.
- Comprehensive user documentation, including detailed specifications and a system integration guide.

**CAST**  
info@cast-inc.com  
www.cast-inc.com

CAST, Inc. 11 Stonewall Court  
Woodcliff Lake, NJ 07677 USA  
tel 201-391-8300 fax 201-391-8694  
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The LJPEG-E core is sourced from  
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