

CAST



LJPEG-E

Lossless JPEG Encoder Core

The LJPEG-E core implements the Lossless JPEG (LJPEG) compression in a compact, high-performance, stand-alone package ideal for applications where bit-by-bit accurate reproduction of an image is essential.

The LJPEG-E conforms to the spatial (sequential) lossless encoding mode (SOF3) of the ISO/IEC 10918-1 standard (CCITT T.81 recommendation). Rather than the Discrete Cosine Transform (DCT) functions used for lossy JPEG compression - which can introduce round-off errors - the LJPEG-E employs a predictor function as described in the specification. It thus encodes and compresses images with no information loss, and requires a significantly smaller physical implementation.

Evaluation designs show that the core fits in a variety of Xilinx devices, requiring, for example, about 1,101 slices for Spartan-6. Its heavily optimized architecture also enables very high performance, reaching up to 245 MSamples/sec with Virtex-6.

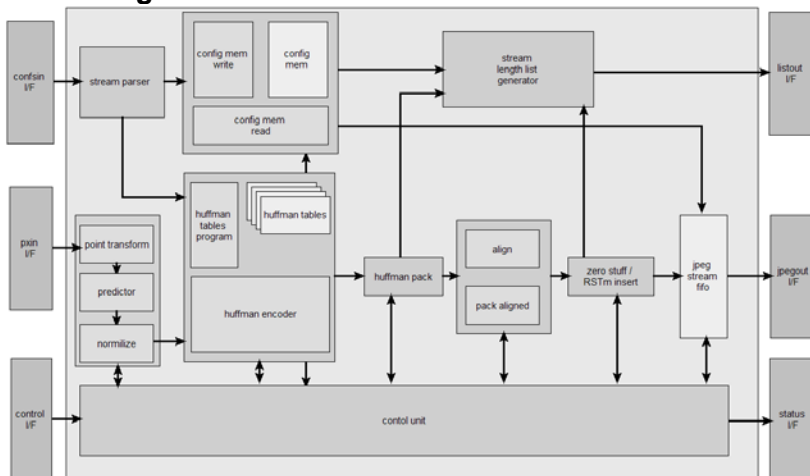
The LJPEG-E is a fully synchronous, strictly positive-edge design with no internal three-state buffers. Comprehensive documentation and a complete verification environment - including a bit-accurate model - help designers integrate and verify the core.

Applications

The LJPEG-E provides a fast, economical solution whenever lossless image compression is essential, including applications such as:

- Medical, military, and space imaging.
- Professional, studio-quality cameras and editing suites.
- High-end film and photo scanners.
- Industrial machine vision systems.

Block Diagram



Features

- Conforms to the spatial (sequential) lossless mode (SOF3) of the ISO/IEC 10918-1 standard (CCITT T.81 recommendation).
- Standalone operation.
 - Pixel samples input.
 - Standalone ISO/IEC 10918-1 JPEG stream output.
- Easily programmable through standard JPEG markers stream.
 - Programmable image dimensions.
 - Full range sample precision support (2 to 16 bits per sample)
 - Up to four programmable Huffman tables.
 - Programmable Restart Interval.
 - Programmable Point Transform function.
 - Programmable APPn and COM markers.
 - Programming errors catch-up features.
- Compact, high-performance architecture.
 - Easily fits most Xilinx device families (see implementation results table).
 - Achieves up to 245 MSamples/sec (Virtex-6).
- Robust and simple to use
 - General purpose, fully stallable, streaming I/O interfaces.

Limitations with respect to the ISO/IEC 10918-1 standard:

- Up to three image-components are supported (Nf field of the SOF3 marker segment = 1 or 2 or 3).
- Single scan encoding (only one SOS marker segment, with Ns field = Nf).
- No DNL marker insertion (Y field of the SOF3 marker segment > 0).
- Fixed parameters.
 - No sub-sampling (Hi and Vi fields of the SOF3 marker segment = 1).
 - Prediction function is fixed to the left-hand predictor, predictor 1. (Ss field of SOS marker segment = 1).

Functional Description

Lossless JPEG was added to the ITU-T JPEG recommendations in 1995. The JPEG lossless mode of operation does not use the 2D-DCT that is used in the lossy mode, since round-off errors prevent a 2D-DCT calculation from being lossless. For the same reason, one would not normally use color space conversion or down-sampling, although these are permitted by the standard.

The lossless mode of the standard codes the difference between each pixel and the "predicted" value for the pixel. The predicted value is a function of the already-transmitted pixels just above and to the left of the current one (eight different predictor functions are defined in the standard). The sequence of the calculated differences (prediction errors) is encoded using the same back end (Huffman or arithmetic) used in the lossy mode. The LJPEG-E core implements the predictor 1 function of the standard, and the Huffman coding back end.

The LJPEG-E core is initially configured using standard JPEG marker segments from the configuration stream input interface. It is configured for frame properties using a standard SOF3 marker segment. Huffman tables that will be used for encoding are programmed through one or more DHT segments. If the restart interval and/or point transform functions are required, they are programmed through the standard DRI and SOS marker segments respectively. If the application needs to use comment and/or application markers, then these are programmed using COM and/or APPn segments and the LJPEG-E will include them in the output stream.

Following initial configuration, the LJPEG-E is ready to accept and encode image frames. Pixel data are written to the core through the pixel input interface and the compressed data are output through the JPEG stream output interface. Configuration can remain constant between consecutive frames or it can change to meet specific frame requirements. In the compressed output stream, the LJPEG-E includes all the necessary markers so that the produced stream is a full, standalone JPEG stream that can be decoded by any ISO/IEC 10918-1 compliant lossless JPEG decoder.

Implementation Results

LJPEG-E core has been evaluated in a variety of technologies. The following are sample Xilinx results using balanced area/speed constraints during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

Xilinx Device	Slices	Fmax (MHz)	I/O	BRAM	Special Features	ISE
Spartan-3 3S1000-5	2,041	90	131	2 RAMB16	-	12.2
Spartan-6 6SLX9-3	1,101	120	131	2 RAMB16	-	12.2
Virtex-5 5VLX30-3	617	190	131	2 RAMB36	-	12.2
Virtex-6 6VLX75T-3	792	245	131	2 RAMB36	-	12.2

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide.

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The LJPEG-E core is sourced from
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