JPEGLS-E

JPEG-LS Encoder Core

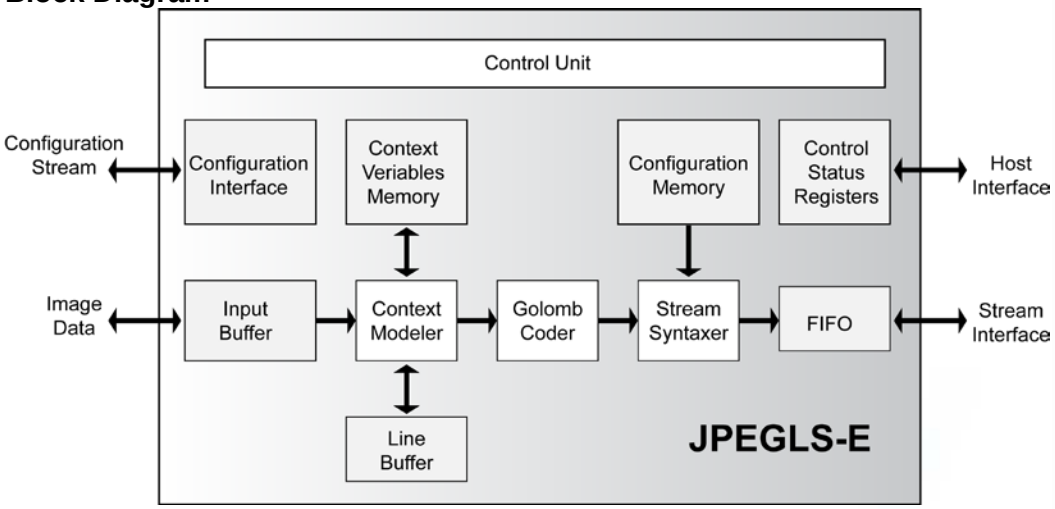
The JPEGLS-E core is a JPEG-LS encoder that forms a high performance solution for image and video lossless compression applications. Providing processing rates up to 161 MSamples/sec on FPGA, a single instantiation of JPEGLS-E suffices for the processing of high rate applications such as HDTV. Compliance with the ISO/IEC 14495-1 JPEG standard makes the JPEG-LS encoder core ideal for any cross platform application such as professional cameras, medical and satellite imaging systems. The core is originally provided with FIFO-like pixel and stream input /output interfaces, but other standard interfaces (e.g. AMBA) are also available. Being carefully designed, and rigorously verified, the JPEGLS-E is a reliable and easy-to-integrate core. Ease of integration is served by a complete verification environment, and additional aids for system on chip simulation.

Applications

The JPEGLS-E can be utilized in a variety of image and video lossless compression encoder applications including:

- Medical imaging
- Satellite imaging
- Professional digital cameras

Block Diagram



Features

ISO/IEC 14495-1 JPEG-LS Compliance

- Programmable local gradient thresholds and context parameters reset threshold value (up to 64)
- Grayscale or 3 component images
- 4:4:4, 4:2:2, 4:1:1 and 4:2:0 sub-sampling formats
- Supports only single scan encoding
- Any image size from 4 x 4 up to 64k x 64k
- 2 up to 16 bits per sample

Ease of Integration

- Single clock per input sample encoding
- Programmable through standard JPEG-LS stream marker segments (supporting SOI, SOF55, SOS, LSE, EOI, APPn and COM)
- Automatic headers generation
- Automatic program-once encode-many operation

Design Quality

- Robust verification
- Scan-ready design

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Functional Description

The JPEGLS-E is configured by feeding it with JPEG headers containing image format and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the JPEGLS-E in raster scan order. Consuming a single clock cycle per image sample, the JPEGLS-E can address the most demanding frame-based video compression applications. The JPEGLS-E outputs a complete JPEG-LS compliant data stream, including JPEG-LS headers.

Implementation Results

JPEGLS-E reference designs have been evaluated in a variety of technologies. The following sample pre-layout results, are reported from a synthesis toll and silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip, for maximum line of 1024 8-bit samples for 3-component images.

ASIC Technology	Logic Eq. Gates	Frequency	Memory
UMC 0.18µ process	58,137	360 MHz	102,076 bits
TSMC 0.09µ process	51,506	700 MHz	102,076 bits

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. The core is silicon proven in FPGA technologies.

Deliverables

The core includes everything required for successful implementation. The ASIC version includes:

- RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Bit-Accurate Model
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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Alma Technologies
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