

CAST



JPEGLS-E

JPEG-LS Encoder Core

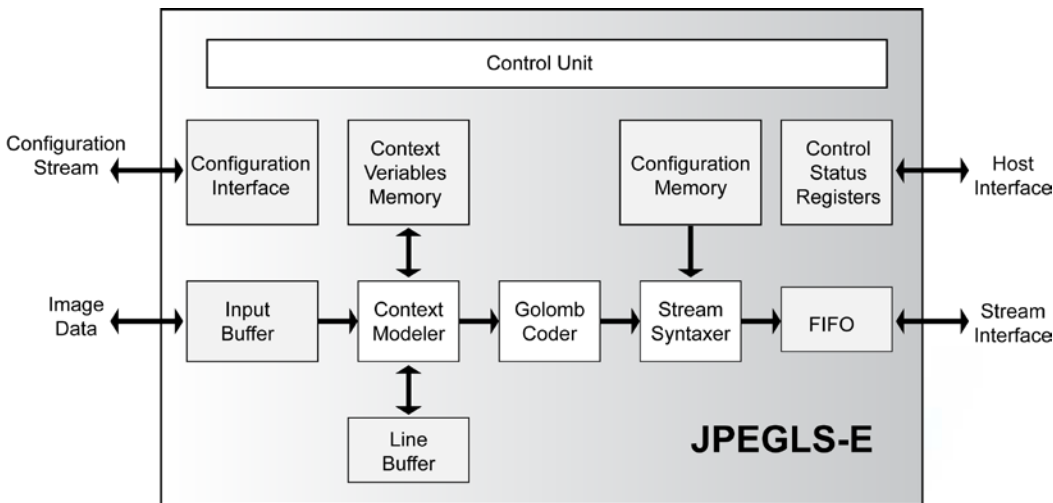
The JPEGLS-E core is a JPEG-LS encoder that forms a high performance solution for image and video lossless compression applications. Providing processing rates up to 190 MSamples/sec on FPGA, the JPEGLS-E suffices for the processing of high rate applications such as HDTV. Compliance with the ISO/IEC 14495-1 JPEG standard makes the JPEG-LS encoder core ideal for any cross platform application such as professional cameras, medical and satellite imaging systems. The core is provided with FIFO-like pixel and stream input /output interfaces. Being carefully designed, and rigorously verified, the JPEGLS-E is a reliable and easy-to-integrate core. Ease of integration is served by a complete verification environment, and additional aids for system on chip simulation.

Applications

The JPEGLS-E can be utilized in a variety of image and video lossless compression encoder applications including:

- Medical imaging
- Satellite imaging
- Professional digital cameras

Block Diagram



Features

ISO/IEC 14495-1 JPEG-LS Compliance

- Programmable local gradient thresholds and context parameters reset threshold value (up to 64)
- Grayscale or 3 component images
- 4:4:4, 4:2:2, 4:1:1 and 4:2:0 sub-sampling formats
- Supports only single scan encoding
- Any image size from 4 x 4 up to 64k x 64k
- 2 up to 16 bits per sample

Ease of Integration

- Single clock per input sample encoding
- Programmable through standard JPEG-LS stream marker segments (supporting SOI, SOF55, SOS, LSE, EOI, APPn and COM)
- Automatic headers generation
- Automatic program-once encode-many operation

Design Quality

- FPGA proven in multiple designs
- Easily fits most Xilinx device families (see implementation results table)

Functional Description

The JPEGLS-E is configured by feeding it with JPEG headers containing image format and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the JPEGLS-E in raster scan order. Consuming a single clock cycle per image sample, the JPEGLS-E can address the most demanding frame-based video compression applications. The JPEGLS-E outputs a complete JPEG-LS compliant data stream, including JPEG-LS headers.

Implementation Results

JPEGLS-E reference designs have been evaluated in a variety of technologies. The following are sample utilization metrics for supporting 24-bit/pixel color images, with up to 2048 pixels/line resolution, in Xilinx devices. Implementation figures are obtained after speed optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

Xilinx Device	Slices	Fmax (MHz)	I/O	BRAM	Special Features	ISE
Spartan-3 3S1000-5	3,917	66	89	20 RAMB16	-	12.2
Spartan-6 6SLX16-3	2,191	95	89	20 RAMB16	-	12.2
Virtex-5 5VLX30-3	1,610	125	89	7 RAMB36 3 RAMB18	-	12.2
Virtex-6 6VLX75T-3	2,202	190	89	7 RAMB36 6 RAMB18	-	12.2

Xilinx Device	Slices	Fmax (MHz)	I/O	BRAM	Special Features	ISE
Spartan-3 3S1000-5	3,917	66	89	20 RAMB16	-	12.2
Spartan-6 6SLX16-3	2,191	95	89	20 RAMB16	-	12.2
Virtex-5 5VLX30-3	1,610	125	89	7 RAMB36 3 RAMB18	-	12.2
Virtex-6 6VLX75T-3	2,202	190	89	7 RAMB36 6 RAMB18	-	12.2

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. The JPEGLS-E has been silicon proven in FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide