The JPEGLS-E core is a standalone and high-performance JPEGLS encoder for lossless still image and video compression applications. The core implements the ISO-14495-1/ITU-T.87 standard, which is based on the low complexity and highly efficient LOCO-I algorithm.

The JPEGLS-E delivers leading lossless compression efficiency on a highly efficient hardware architecture. A single instantiation of the core can encode full-HD or higher rates, even in low-cost FPGAs. It is originally provided with FIFO-like pixel and stream input/output interfaces, but other standard interfaces (e.g. AMBA/AHB) are also available. Being carefully designed, rigorously verified, and production-proven, the JPEGLS-E is a reliable and easy-to-integrate core. Ease of integration is served by a complete verification environment, including a bit-accurate software model.

Applications
The JPEGLS-E can be utilized in a variety of image and video lossless compression encoder applications including:
- Medical imaging
- Satellite imaging
- Professional digital cameras

Block Diagram

**Features**

ISO/IEC 14495-1 JPEGLS Compliance
- Any image size from 8 x 8 up to 64k x 64k
- Grayscale, 4:4:4, 4:2:2, 4:1:1 and 4:2:0 sub-sampling formats
- 2 up to 16 bits per sample
- Programmable point transform
- Programmable local gradient thresholds and context parameters reset threshold value (up to 64)

Smooth System Integration
- Single clock per input sample encoding
- Programmable through standard JPEGLS marker segments
- Automatic headers generation
- Automatic program-once encode-many operation
- Simple, microcontroller like, programming interface
- Flow controllable, streaming-capable Avalon-ST™ I/O data interfaces

Easy Verification and Technology Mapping
- Extensive documentation
- Bit Accurate Model (BAM) and Test Vector generator
- Self checking testbench environment
- Sample scripts
- Fully portable HDL source code
- No internal tri-states
- Scan-ready design
- Strictly positive edge triggered design using D-type
- only Flip-Flops
- Fully synchronous operation
No need for special timing constraints
Functional Description

The JPEGLS-E is configured by feeding it with JPEG headers containing image format and encoding options data. The core’s configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the JPEGLS-E in raster scan order. Consuming a single clock cycle per image sample, the JPEGLS-E can address the most demanding frame-based video compression applications. The JPEGLS-E outputs a complete JPEG-LS compliant data stream, including JPEG-LS headers.

Implementation Results

JPEGLS-E reference designs have been evaluated in a variety of technologies. The following are sample Actel results.

<table>
<thead>
<tr>
<th>Actel Device</th>
<th>Cells</th>
<th>RAM Blocks</th>
<th>I/Os</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTAX</td>
<td>3605</td>
<td>9060</td>
<td>19</td>
<td>41</td>
</tr>
<tr>
<td>RTAX2000S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ProASIC3</td>
<td>3643</td>
<td>15209</td>
<td>19</td>
<td>45</td>
</tr>
<tr>
<td>A3P1000-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. The core is silicon proven in FPGA technologies.

Deliverables

The core includes everything required for successful implementation. The Actel version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench (Verilog versions use Verilog 2001)
- Verilog and Bit-Accurate Model
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide