The JPEGLS-E core is a standalone and high-performance JPEGLS encoder for lossless still image and video compression applications. The core implements the ISO-14495-1/ITU-T.87 standard, which is based on the low complexity and highly efficient LOCO-I algorithm.

The JPEGLS-E delivers leading lossless compression efficiency on a highly efficient hardware architecture. A single instantiation of the core can encode full-HD or higher rates, even in low-cost FPGAs. It is originally provided with FIFO-like pixel and stream input/output interfaces, but other standard interfaces (e.g. AMBA/AHB) are also available. Being carefully designed, rigorously verified, and production-proven, the JPEGLS-E is a reliable and easy-to-integrate core. Ease of integration is served by a complete verification environment, including a bit-accurate software model.

Applications
The JPEGLS-E can be utilized in a variety of image and video lossless compression encoder applications including:
- Medical imaging
- Satellite imaging
- Professional digital cameras

Block Diagram
Functional Description

The JPEGLS-E is configured by feeding it with JPEG headers containing image format and encoding options data. The megafuction's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the JPEGLS-E in raster scan order. Consuming a single clock cycle per image sample, the JPEGLS-E can address the most demanding frame-based video compression applications. The JPEGLS-E outputs a complete JPEG-LS compliant data stream, including JPEG-LS headers.

Implementation Results

JPEGLS-E reference designs have been evaluated in a variety of technologies. The following are sample Altera results for maximum line of 1024 8-bit samples for 3-component images. Implementation figures are obtained after speed optimization during synthesis and place and route, while assuming that all megafuction I/Os are routed off-chip.

<table>
<thead>
<tr>
<th>Altera Device</th>
<th>Logic</th>
<th>Frequency</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone EP1C12-6</td>
<td>10,673 LEs</td>
<td>80 MHz</td>
<td>29 M4K</td>
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<tr>
<td>Cyclone-II EP2C20-6</td>
<td>10,894 LEs</td>
<td>99 MHz</td>
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<tr>
<td>Cyclone-III EP3C10-6</td>
<td>8,867 LEs</td>
<td>100 MHz</td>
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<td>Stratix EP1S20-6</td>
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<tr>
<td>Stratix-II EP2S15-3</td>
<td>9,875 ALUTs</td>
<td>102 MHz</td>
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<td>Hardcopy-II HC210 -6</td>
<td>45,535 HCells</td>
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</table>

Support

The megafuction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafuction has been verified through extensive simulation and rigorous code coverage measurements. The megafuction is silicon proven in FPGA technologies.

Deliverables

The megafuction includes everything required for successful implementation. The Altera version includes:
- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench (Verilog versions use Verilog 2001)
- Bit-Accurate Model
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide