JPEG2RTP

Hardware RTP Stack for JPEG Stream Encapsulation

Implements a Real Time Transport Protocol (RTP) hardware stack that encapsulates JPEG streams to RTP packets compliant with RFC 2435.

The JPEG2RTP can be directly connected to the output of a JPEG encoder to output RTP packets, which can subsequently be forwarded for UDP/IP or TCP/IP encapsulation. The hardware stack produces complete RTP packets, without the need for any host-processor assistance. Along with CAST's UDP/IP hardware stack, the JPEG2RTP core is ideal for offloading the demanding task of RTP/UDP/IP encapsulation from a host processor, and enables JPEG video streaming even in processor-less SoC designs.

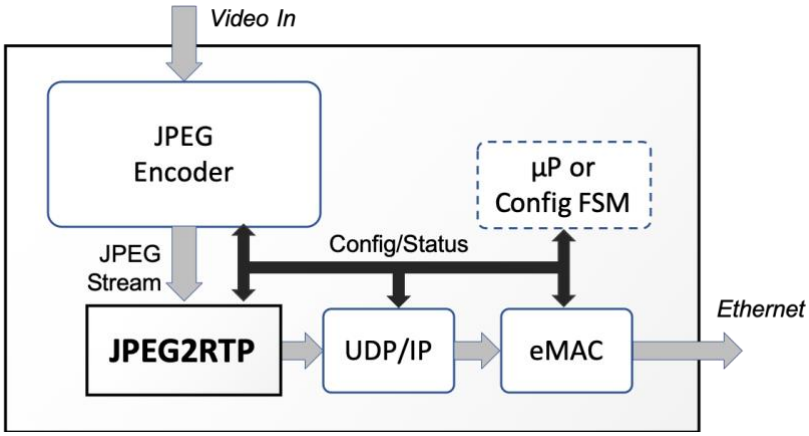
The core is easy to integrate in systems with or without a host processor. JPEG stream and RTP packet data can are input/output via dedicated streaming-capable AXI4-Stream or Avalon-ST interfaces, enabling direct connection to hardware video encoders and hardware stacks for UDP or TCP. Status and control registers are accessible by AXI4-Lite or Avalon-MM interface.

The JPEG2RTP core is available in RTL source or as a targeted FPGA netlist. Platforms integrating the core with JPEG encoder, UDP/IP, and eMAC cores, are also available from CAST, and can enable rapid development of video over IP systems.

Applications

The JPEG2RTP core is suitable for a wide variety of systems and devices featuring JPEG video streaming over IP networks. A sample block diagram of such systems is provided below.

Block Diagram



FEATURES

RTP Encapsulation for JPEG Streams

- Compliant to RFC 2435
- Enables control of RTP packet size
  - Run-time programmable maximum stream bytes per RTP packet
  - In-band Quantization Table support

Easier Integration for Faster Development

- Processor-less, standalone operation
- AMBA® - AXI Interfaces
  - AXI4-Lite Control/Status register interfaces
  - AXI4-Streaming interfaces for packet data
- Avalon Interfaces
  - Avalon-MM Control/Status register interfaces
  - Avalon-ST interfaces for packet data
- Available pre-integrated with:
  - JPEG Encoder cores from CAST
  - UDP/IP Hardware Stack from CAST
  - Altera, Xilinx, or other third-party eMAC core

Support

The JPEG2RTP as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Related Products

- JPEG Baseline/Extended/Ultra-Fast Encoder Cores
- UDPIP: UDP/IP Hardware Protocol Stack Core

CAST

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