The JPEG2K-E core is a complete high performance JPEG2000 - ISO/IEC 15444-1 image compression solution targeted for video and high bandwidth image compression applications.

The JPEG2k-E core delivers real JPEG2000 compression efficiency. Commonly used hardware simplification compromises, such as bypass and parallel mode of the entropy coding process, that damage the JPEG2000 rate-distortion efficiency have not been adopted. Furthermore, the core implements an accurate rate-control that delivers quality practically equivalent to de-facto software encoders. Region of interest coding, progressive streams with multiple quality layers, lossy and lossless compression are JPEG2000 standard benefits also delivered from the JPEG2k-E core.

A single JPEG2k-E core provides processing rates higher than 130 MSamples/sec. Users of the core can use parallel instantiations to meet the processing rate requirements even of the most demanding applications.

The JPEG2K-E is a reliable and easy-to-integrate core as it is carefully designed, rigorously verified, and production proven. The architecture can be fine-tuned based on the application specific needs. Ease of integration is served by a complete verification environment, and additional aids for system on chip simulation, such as a software bit-accurate model.

Block Diagram
Applications
- Digital still cameras and camcorders
- Networked video (Motion JPEG 2000) and image distribution systems
- Wireless video and image distribution systems
- Digital CCTV and surveillance systems
- Image/Video editing systems
- Medical imaging - DICOM
- Military/Aerospace imaging systems

Functional Description
The JPEG2K-E operates either on an entire image or on a rectangular section of an image called a tile. The maximum supported image/tile size depends on the size of the external memory, while provided enough external memory the core can support up to 65,535x65,535 images, and up to 8,192x8,192 tiles.

In terms of internal operation, the input pixels are first level-shifted and then transformed using either the reversible 5/3 or the irreversible 9/7 two-dimensional discrete wavelet transform; the transformed coefficients are stored in the external memory. After an entire tile has been transformed, the transformed coefficients are quantized; the quantized coefficients are fed to the Entropy Coding Engines in a code-block per code-block basis.

The coded-segments along with the code-block attributes (truncation lengths and distortion metrics) produced by the Entropy Coding Engines are fed to the Rate Control Engine. If enabled, the Rate Control Engine implements a proprietary PCRD algorithm that outputs code-stream at the required compression ratio with the minimum possible quality loss. The JPEG2K-E core can optionally support multiple quality layers, in which case the user can program the desired compression ratio per each quality layer. Finally the Headers-Syntax Unit forms global, tile and packet headers, and outputs a compliant stream or file.

Verification
The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies. Evaluation boards are available upon request.

Implementation Results
The silicon requirements and the maximum sustained throughput of the JPEG2K-E depend strongly on the selected configuration of the core and on the available external memory bandwidth. The following sample Xilinx implementation figures are indicative of the JPEG2K-E core capabilities and their corresponding utilization metrics

<table>
<thead>
<tr>
<th>Xilinx Device</th>
<th>Slices</th>
<th>Fmax (MHz)</th>
<th>Throughput (MSamples/s)</th>
<th>BRAM</th>
<th>DSP48</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex7 XC7V330T-3</td>
<td>15,217</td>
<td>230</td>
<td>145</td>
<td>48 Ramb36 67 Ramb18</td>
<td>61</td>
</tr>
<tr>
<td>Spartan-6 6SLX150-3</td>
<td>18,030</td>
<td>66</td>
<td>42</td>
<td>103 Ramb16</td>
<td>56</td>
</tr>
<tr>
<td>Virtex6 6VXL130T-3</td>
<td>13,704</td>
<td>210</td>
<td>130</td>
<td>32 Ramb36 89 Ramb18</td>
<td>55</td>
</tr>
<tr>
<td>Virtex-5 5VXL155-3</td>
<td>15,400</td>
<td>190</td>
<td>120</td>
<td>32 Ramb36 89 Ramb18</td>
<td>55</td>
</tr>
<tr>
<td>Virtex-5 5VXL130T-1</td>
<td>14,965</td>
<td>140</td>
<td>88</td>
<td>32 Ramb36 89 Ramb18</td>
<td>55</td>
</tr>
<tr>
<td>Virtex-5Q XQ5VFX130T-1</td>
<td>16,710</td>
<td>140</td>
<td>88</td>
<td>32 Ramb36 89 Ramb18</td>
<td>55</td>
</tr>
<tr>
<td>Virtex-5QV Resources utilization and speed are approximately equivalent to those for Virtex-5 (-1) and Virtex-5Q (-1).</td>
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Support
The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables
The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:
- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench
- (Software (C++) Bit accurate model and test vector generator
- Simulation scripts, test vectors, and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Cores
- DDR/DDR2 SDRAM Memory Controller IP core
- AES encryption IP cores
- CMMI (Multimedia Interface with DMA for AHB bus) core
- PCI and PCI Express IP cores