

CAST



JPEG2K-E

JPEG 2000 Encoder Core

Features

JPEG 2000 compliance

- Both lossless and lossy compression
- Error-resilient compression
- Rate control
- Headers syntax processing (JPC, JP2, proprietary)

Real JPEG2000 Performance

- No hardware simplification compromises
- Not based on bypass and parallel mode of entropy coding
- High-quality, accurate rate-control
- Region Of Interest

Flexible Input Image Format

- All widely used sub-sampling formats (e.g. 444, 422, etc)
- Image up to 65,535x65,535
- Tile size up to 8,192x8,192
- Up to 4 color components
- 8 up to 16 bits per sample

Programmable JPEG2000 options

- 2D-DWT filter type (5/3 or 9/7)
- Number of 2D-DWT levels
- Quantization tables
- Entropy-coding switches
- Code-block size (64 or 32 or 16 on each dimension)
- Up to 30 quality layers
- Compression ratio per quality layer
- CPRL and LRCP (grayscale only) progression
- Region Of Interest size

Tunable architecture during synthesis

- Configurable number of entropy coding engines
- Configurable maximum image/tile size

Flexible Interfaces

- 16-bit synchronous SRAM-style host interface
- Dedicated pixel-in and stream-out interfaces
- Independent of external memory type (DDR2/3, SDRAM, SRAM, etc.)
- Glue-less connection to Xilinx and CAST memory controllers

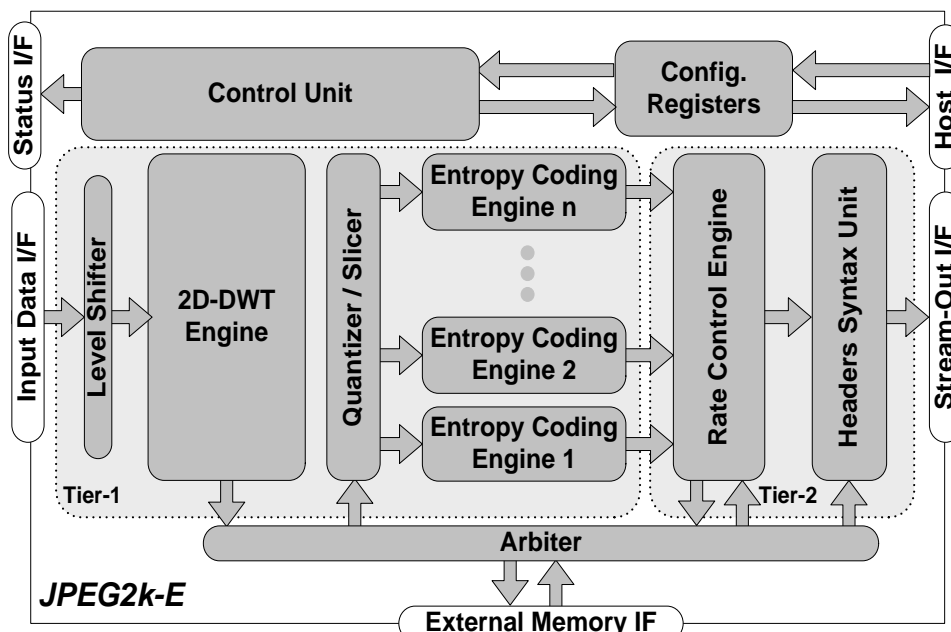
The JPEG2K-E core is a complete high performance JPEG2000 - ISO/IEC 15444-1 image compression solution targeted for video and high bandwidth image compression applications

The JPEG2k-E core delivers real JPEG2000 compression efficiency. Commonly used hardware simplification compromises, such as bypass and parallel mode of the entropy coding process, that damage the JPEG2000 rate-distortion efficiency have not been adopted. Furthermore the core implements an accurate rate-control that delivers quality practically equivalent to de-facto software encoders. Region of interest coding, progressive streams with multiple quality layers, lossy and lossless compression are JPEG2000 standard benefits also delivered from the JPEG2k-E core.

A single JPEG2k-E core provides processing rates higher than 130 MSamples/sec. Users of the core can use parallel instantiations to meet the processing rate requirements even of the most demanding applications.

The JPEG2K-E is a reliable and easy-to-integrate core as it is carefully designed, rigorously verified, and production proven. The architecture can be fine-tuned based on the application specific needs. Ease of integration is served by a complete verification environment, and additional aids for system on chip simulation, such as a software bit-accurate model.

Block Diagram



Applications

- Digital still cameras and camcorders
- Networked video (Motion JPEG 2000) and image distribution systems
- Wireless video and image distribution systems
- Digital CCTV and surveillance systems
- Image/Video editing systems
- Medical imaging - DICOM
- Military/Aerospace imaging systems

Functional Description

The JPEG2K-E operates either on an entire image or on a rectangular section of an image called a tile. The maximum supported image/tile size depends on the size of the external memory, while provided enough external memory the core can support up to 4096x4096 images.

In terms of internal operation, the input pixels are first level-shifted and then transformed using either the reversible 5/3 or the irreversible 9/7 two-dimensional discrete wavelet transform; the transformed coefficients are stored in the external memory. After an entire tile has been transformed, the transformed coefficients are quantized; the quantized coefficients are fed to the Entropy Coding Engines in a code-block per code-block basis.

The coded-segments along with the code-block attributes (truncation lengths and distortion metrics) produced by the Entropy Coding Engines are fed to the Rate Control Engine. If enabled, the Rate Control Engine implements a proprietary PCRD algorithm that outputs code-stream at the required compression ratio with the minimum possible quality loss. The JPEG2K-E core can optionally support multiple quality layers, in which case the user can program the desired compression ratio per each quality layer. Finally the Headers-Syntax Unit forms global, tile and packet headers, and outputs a compliant stream or file.

Related Cores

- DDR/DDR2 SDRAM Memory Controller IP core
- AES encryption IP cores
- CMMI (Multimedia Interface with DMA for AHB bus) core
- PCI and PCI Express IP cores

Implementation Results

The silicon requirements and the maximum sustained throughput of the JPEG2K-E depend strongly on the selected configuration of the core and on the available external memory bandwidth. The following sample Xilinx implementation figures are indicative of the JPEG2K-E core capabilities and their corresponding utilization metrics

Xilinx Device	Slices	Fmax (MHz)	Throughput (MSamples/s)	BRAM	DSP48
Spartan-6 6SLX150-3	18,030	66	42	103 RAMB16	56
Virtex-5 5VLX155-3	15,400	190	120	32 RAMB36 53 RAMB18	55
Virtex-6 6VLX130T-3	13,704	210	130	32 RAMB36 89 RAMB18	55

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies. Evaluation boards are available upon request.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench
- (Software (C++)) Bit accurate model and test vector generator
- Simulation scripts, test vectors, and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide