

# CAST



## JPEG2K-E

### JPEG 2000 Encoder Core

The JPEG2K-E core is a complete high performance JPEG2000 - ISO/IEC 15444-1 image compression solution targeted for video and high bandwidth image compression applications

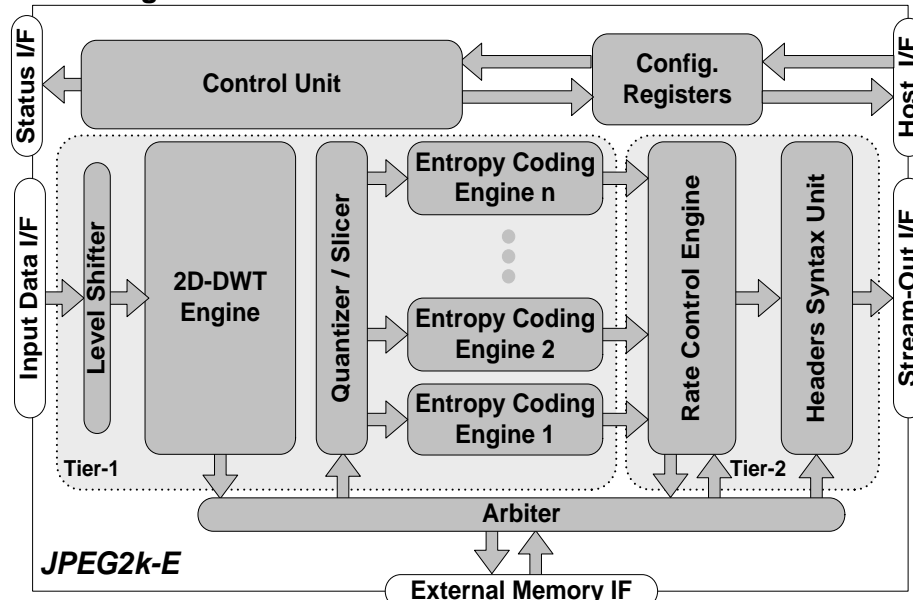
Implementing in custom hardware tier-1 and tier-2 encoding (including rate control), the core once programmed can receive pixel data and output fully compliant stream at the desired compression ratio. Furthermore, being able to support frame/tile sizes up to 4096 x 4096 pixels, and providing processing rates up to 150 MSamples/sec, JPEG2K-E eliminates the need for parallel processing even for the most demanding application such as HDTV.

The JPEG2K-E is a reliable and easy-to-integrate core as it is carefully designed, and rigorously verified. The architecture can be fine-tuned based on the application specific needs. Ease of integration is served by a complete verification environment, and additional aids for system on chip simulation, such as a software bit-accurate model.

### Applications

- Digital still cameras and camcorders
- Networked video (Motion JPEG 2000) and image distribution systems
- Wireless video and image distribution systems
- Digital CCTV and surveillance systems
- Image/Video editing systems
- Satellite imaging
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### Block Diagram



### Features

#### JPEG 2000 compliance

- Both lossless and lossy compression
- Error-resilient compression
- Rate control
- Headers syntax processing

#### Flexible Input Image Format

- 4 component input supporting all widely used sub-sampling formats (e.g. 444, 422, 420, 411 and grayscale)
- Image/Tile size up to 4096x4096 adds flexibility to external memory requirements
- Up to 4 color components
- 8 to 16 bits per sample

#### Output format

- Proprietary attributes/coded data format
- Standard compliant stream (.jpc)
- Standard compliant file (.jp2)

#### Programmable JPEG2000 options

- 2D-DWT filter type (5/3 or 9/7)
- Number of 2D-DWT levels
- Quantization tables
- Entropy-coding switches (reset, restart, segmark)
- Input format (pixel depth, image and tile size, number of color components, sub-sampling factors)
- Code-block size (64 or 32 or 16 on each dimension)
- Up to 30 quality layers
- Compression ratio per quality layer
- CPRL and LRCP (grayscale only) progression

#### Tunable architecture during synthesis

- Configurable number of entropy coding engines
- Configurable maximum image/tile size

#### Flexible Interfaces

- 16-bit synchronous SRAM-style host interface
- Dedicated pixel-in and stream-out interfaces (Avalon Streaming)
- Independent of external memory type (DDR2/3, SDRAM, SRAM, etc.)

## Features Continued

- Pin-compatible with CAST's & Xilinx's memory controller
- Optional OCP wrapper
- Fully synchronous single-clock domain design

## Functional Description

The JPEG2K-E operates either on an entire image or on a rectangular section of an image called a tile. The maximum supported image/tile size depends on the size of the external memory, while provided enough external memory the core can support up to 4096x4096 images.

Synthesis and run-time parameters allow customization of the core for compression performance, area speed and memory trade-offs.

In terms of internal operation, the input pixels are first level-shifted and then transformed using either the reversible 5/3 or the irreversible 9/7 two-dimensional discrete wavelet transform; the transformed coefficients are stored in the external memory. After an entire tile has been transformed, the transformed coefficients are quantized; the quantized coefficients are fed to the Entropy Coding Engines in a code-block per code-block basis.

The coded-segments along with the code-block attributes (truncation lengths and distortion metrics) produced by the Entropy Coding Engines are fed to the Rate Control Engine. If enabled, the Rate Control Engine implements a proprietary PCRD algorithm that outputs code-stream at the required compression ratio with the minimum possible quality loss. The JPEG2K-E core can optionally support multiple quality layers, in which case the user can program the desired compression ratio per each quality layer. Finally the Headers-Syntax Unit forms global, tile and packet headers, and outputs a compliant stream or file.

The design is fully synchronous with a single-clock domain.

## Implementation Results

The processing speed and area requirements of the JPEG2K-E heavily depend on the synthesis configuration as well as the external memory bandwidth. The following Xilinx implementation data are indicative of the JPEG2K-E core capabilities and resources requirements.

Device	External Memory	Video Format	Frames/sec
Virtex-4 (xc4v160 or higher)	32 Mbytes	1080p (4:2:0)	30
Virtex-5 (xc5vlx155 or higher)	16 Mbytes	1080p (4:2:2)	25

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies. Hardware evaluation boards are available upon request.

## Deliverables

The core includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist (VHDL RTL optional)
- Sophisticated self-checking HDL Testbench including everything needed to test the core
- Bit accurate model in C++
- Simulation scripts, vectors, and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

## Associated IP Cores

- DDR/DDR2 SDRAM Memory Controller IP core
- AES encryption IP cores
- PCI and PCI Express IP cores
- CMMI (Multimedia Interface with DMA for AHB bus) core