



JPEG-LS-D

Lossless & Near-Lossless
JPEG-LS Decoder

Features

JPEG-LS Standard Support

- All JPEG-LS encoding parameters
- Optional Near Lossless support
- All interleaved modes
- All marker segments including APP, COM, DNL and Restart markers
- Image resolution, higher than 64Kx64K (supports oversize image dimension parameters)
- Up to 16 bits per color sample, and up to 4 color components

Easy to Use and Integrate

- Requires no programming or control from host
- Reports image format
- Detects and reports marker syntax errors
- Delivered with bit-accurate software model
- AXI4-Stream Interfaces for image and compressed data, and 32-bit wide APB for register access
- Dedicated interface for APP and COM markers to pass metadata to system

Versions and Throughput

- One sample per cycle, for the area optimized JPEG-LS-DS version
 - Up to 55 Msamples/sec on Arria-10 (speed grade 3), and from 3,800 ALMs
- Synthesis configurable number of samples per cycle, for the throughput optimized JPEG-LS-DF version. Maximum throughput is only possible when images are encoded using restart markers.

Deliverables

- Source code RTL (Verilog) or Targeted FPGA Netlist
- Bit Accurate Model
- Sample simulation and synthesis scripts
- Verification testbenches
- Comprehensive documentation

The JPEG-LS-D core implements a highly efficient and low-power, lossless and near-lossless image decompression engine that is compliant to the JPEG-LS, ISO/IEC 14495-1 standard.

The decoder core can decompress any JPEG-LS stream or JPEG-LS payload of image container formats, such as DICOM. It accepts compressed streams of images with up to 16-bit per color sample and up to four color components, in all widely-used color subsampling formats. Supports oversize image dimension parameters, the core can decode image with resolutions exceeding 64k x 64k pixels.

The easy-to-use JPEG-LS-D core operates on a standalone basis, parsing marker segments and decompressing coded data with no assistance from a host processor. The decoder reports the image format (i.e., resolution, subsampling format, and color sample-depth) to the system, so that the decoded images are properly further processed and/or displayed. Application (APP) or comment (COM) marker segments, which are typically used to embed metadata in the compressed stream, are also passed to the system via a dedicated interface.

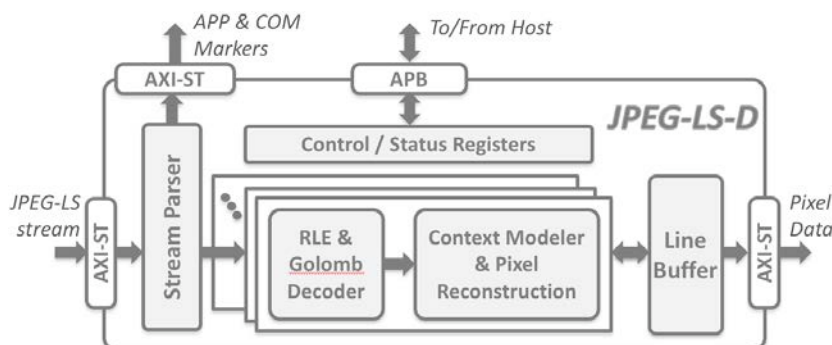
SoC integration is straightforward thanks to standardized AMBA® interfaces. The core accepts compressed data and outputs pixel data, frame format information and APP or COM marker segments via AXI4-Stream interfaces, and it provides access to its control and status registers via a 32-bit APB interface. A wrapper that bridges the AXI-Stream interfaces to AXI4 can optionally be delivered with the core.

The core is designed with industry best practices, and its reliability has been proven through both rigorous verification and silicon validation. The deliverables include a complete verification environment and a bit-accurate software model.

Versions

The core is available in two versions: JPEG-LS-DS and JPEG-LS-DF. JPEG-LS-DS is the core's size-optimized version, which provides a throughput of one sample per cycle, and requires only one image line of buffering. A single JPEG-LS-DS core is capable of decompressing several tens of Msamples per second when mapped on Intel FPGA/s. The JPEG-LS-DF is the scalable-throughput version of the core, which can process multiple samples per cycle by internally aggregating a user-defined number of JPEG-LS-DS cores. The JPEG-LS-DF is suitable for compressing images or video with ultra-high resolutions and/or frame rates but assumes the use of restart markers in the encoded stream.

Block Diagram



Silicon Resources Utilization

The JPEG-LS-D can be mapped to any Intel FPGA device, provided enough silicon resources are available. The size of a core depends on its configuration. The following table provides sample area and performance data for the JPEG-LS-D core mapped on an Arria-10 device (speed grade 3) and excludes the image line buffer.

Core Version	Max. Bits per Sample	Max. NEAR Value	FPGA Resources		MSamples per sec
			ALMs	Mem. Bits	
JPEG-LS-DS	8	0	5,095	25,046	63
		4	5,455	25,046	55
		8	5,535	25,046	50
	10	0	5,503	30,014	61
		4	5,958	30,014	50
		8	5,976	30,014	41
	16	0	7,767	45,283	77
		4	8,479	45,283	37
		8	8,492	45,283	31
JPEG-LS-DF with 3 cores	8	0	12,850	75,208	189
	10		13,824	90,112	183
	16		20,378	135,919	168

Note that the list of core configurations is not exhaustive, and that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please consult with CAST to get accurate characterization data for your target technology and required core configuration.

Deliverables

The core is available in source code RTL (Verilog) or as an FPGA netlist, and its deliverables include everything required for successful implementation:

- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Applications

The JPEG-LS-D is suitable for applications requiring numerically or visually lossless compression of images or video of potentially high color or greyscale accuracy such as medical Imaging (DICOM), aerospace imaging/surveillance and advanced driver assistance systems.

JPEG-LS Compression Efficiency

Despite its lower computational complexity JPEG-LS offers exceptionally high lossless compression efficiency. JPEG-LS is expected to outperform PNG, and to provide similar compression ratios as lossless JPEG2000 for both color and greyscale images. Following are some indicative examples:

