The JPEG-E core is a standalone and high-performance JPEG encoder for still image and video compression applications.

One of the fastest available JPEG encoders, the JPEG-E can encode multiple Full HD channels even in low-cost FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E core ideal for interoperable systems and devices. In addition to generating standalone Baseline JPEG streams, the core is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. The JPEG-E can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the core has a small footprint, requiring, for example, approximately 50,000 equivalent gates and 16kbits of internal memory for a 90nm implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 750 MSamples/sec in a 65nm technology.

The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and silicon-proven, the JPEG-E is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E core is suitable for implementing a variety of digital imaging applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, scanners etc)
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram

Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC)
- Programmable quantization tables (up to four)
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers
- Standalone, Baseline JPEG stream output

Additional Processing Capabilities

- Programmable Quantization Quality (1 to 100)
- Motion JPEG payload encoding
- Rate-Control (optional)
- One-pass compression ratio regulation (optional)
  - Motion JPEG video oriented rate control option with programmable nominal output frame size and transmission buffer size in bytes
  - Block-based, rate control option with independent Luminance and Chrominance thresholds

Designed for Easy Integration

- Simple, microcontroller like, programming interface
- Avalon-ST™ I/O data interfaces
- Optional raster-to-block conversion
- Optional AHB or AXI bus interfaces
- Single clock per input sample processing rate
- Fully programmable through standard JPEG marker segments
- Automatic JPEG markers generation on the output
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The core’s configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are input to the JPEG-E in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-E can address the most demanding image and video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized.

Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following are ASIC pre-layout results reported from synthesis tool and silicon vendor design kit under typical conditions with all core I/Os assumed to be routed on-chip. Implementation numbers are for the core optimized for speed.

<table>
<thead>
<tr>
<th>ASIC Technology</th>
<th>Logic Eq. Gates</th>
<th>Fmax (MHz)</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMC 0.18µ process</td>
<td>54,500</td>
<td>300</td>
<td>16,448 bits</td>
</tr>
<tr>
<td>TSMC 0.18µ process</td>
<td>61,000</td>
<td>300</td>
<td>16,448 bits</td>
</tr>
<tr>
<td>TSMC 90nm process</td>
<td>49,000</td>
<td>500</td>
<td>16,448 bits</td>
</tr>
<tr>
<td>TSMC 65nm process</td>
<td>58,200</td>
<td>750</td>
<td>16,448 bits</td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Synthesis scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Cores

- JPEG-E-X Baseline/Extended Sequential JPEG Encoder – adds support for 12 bits per sample
- SVE-JPEG-E SpeedView Enabled JPEG Encoder that produces SpeedView enabled JPEG data streams.
- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-E core.