

# CAST



## JPEG-E

### Baseline JPEG Encoder Core

#### Features

##### Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC)
- Programmable quantization tables (up to four)
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers
- Standalone, Baseline JPEG stream output

##### Additional Processing Capabilities

- Motion JPEG payload encoding
- Rate-Control (optional)

##### Designed for Easy Integration

- Simple and zero latency streaming interfaces
- Single clock per input sample processing rate
- Fully programmable through standard JPEG marker segments
- Automatic JPEG markers generation on the output
- Automatic program-once encode-many operation

##### Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Easily fits most Xilinx device families (see implementation results table)

The JPEG-E core is a standalone and high-performance JPEG encoder for still image and video compression applications.

One of the fastest available JPEG encoders, the JPEG-E can encode at Full HD (1080p30) or higher rates, even in FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E core ideal for interoperable systems and devices. In addition to generating standalone Baseline JPEG streams, the core is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. The JPEG-E can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the core fits in a variety of Xilinx devices, requiring, for example, approximately 1,400 slices for a Spartan-6 implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 275 MSamples/sec in a Virtex-6 device.

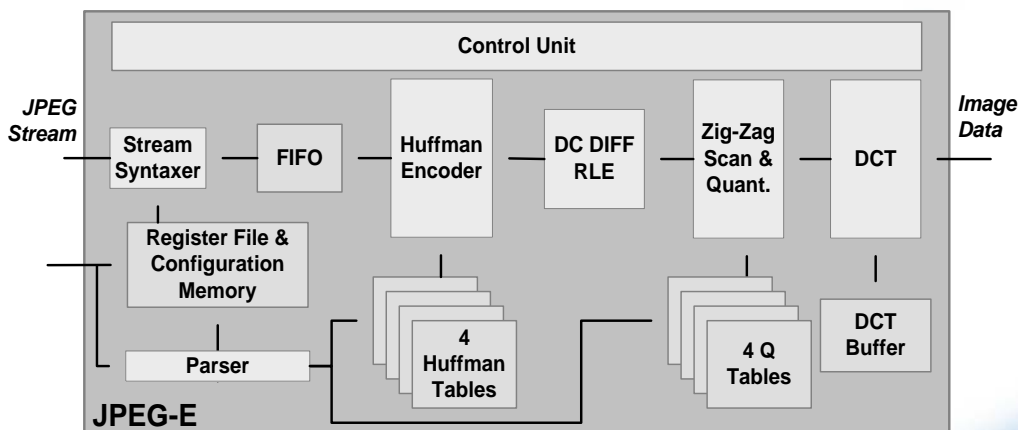
The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and silicon-proven, the JPEG-E is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

## Applications

The JPEG-E core is suitable for implementing a variety of digital imaging applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, scanners etc)
- Medical imaging systems
- Video conference systems
- Surveillance systems

## Block Diagram



## Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The core's configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are input to the JPEG-E in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-E can address the most demanding image and video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized.

## Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following sample Xilinx results are obtained after speed optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

Xilinx Device	Slices	Fmax (MHz)	I/O	BRAM	Special Features	ISE
Spartan-3 3S1000-5	2,445	115	73	7 RAMB16	9 MULT18	12.2
Spartan-6 6SLX9-3	1,343	170	73	7 RAMB16	9 DSP48	12.2
Virtex-5 5VLX30-3	1,068	240	73	1 RAMB36 3 RAMB18	9 DSP48	12.2
Virtex-6 6VLX75T-3	1,250	275	73	1 RAMB36 5 RAMB18	9 DSP48	12.2

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

## Related Cores

- JPEG-E-X Baseline/Extended Sequential JPEG Encoder – adds support for 12 bits per sample
- SVE-JPEG-E SpeedView Enabled JPEG Encoder that produces SpeedView enabled JPEG data streams.
- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-E core.