The JPEG-E core is a standalone and high-performance JPEG encoder for still image and video compression applications.

One of the fastest available JPEG encoders, the JPEG-E can encode at Full HD (1080p30) or higher rates, even in low-cost Cyclone-6 devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E core ideal for interoperable systems and devices. In addition to generating standalone Baseline JPEG streams, the core is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. The JPEG-E can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the core fits in a variety of Xilinx devices, requiring, for example, approximately 1,400 slices for a Spartan-6 implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 350 MSamples/sec in a Virtex-7 device.

The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and silicon-proven, the JPEG-E is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E core is suitable for implementing a variety of digital imaging applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, scanners etc)
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram
Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The core’s configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are input to the JPEG-E in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-E can address the most demanding image and video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized.

Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following sample Xilinx results are obtained after speed optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

<table>
<thead>
<tr>
<th>Xilinx Device</th>
<th>Slices</th>
<th>Fmax (MHz)</th>
<th>BRAM</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-3 3S1000-5</td>
<td>2,445</td>
<td>115</td>
<td>7 RAMB16</td>
<td>9 MULT18</td>
</tr>
<tr>
<td>Spartan-6 6SLX9-3</td>
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<td>170</td>
<td>7 RAMB16</td>
<td>9 DSP48</td>
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<td>Virtex-5 5VLX30-3</td>
<td>1,068</td>
<td>240</td>
<td>1 RAMB36 5 RAMB18</td>
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<td>Virtex-6 6VLX7T-3</td>
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<tr>
<td>Artix-7 7A100T-3</td>
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<td>275</td>
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</tr>
<tr>
<td>Kintex-7 7K70T-3</td>
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<td>1 RAMB36 4 RAMB16</td>
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</tr>
<tr>
<td>Virtex-7 7V330-3</td>
<td>1,505</td>
<td>350</td>
<td>1 RAMB36 4 RAMB16</td>
<td>9 DSP48</td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Cores

- JPEG-E-X Baseline/Extended Sequential JPEG Encoder – adds support for 12 bits per sample
- SVE-JPEG-E SpeedView Enabled JPEG Encoder that produces SpeedView enabled JPEG data streams.
- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-E core.