



JPEG-E

Baseline JPEG Encoder Megafunction

The JPEG-E megafunction is a standalone and high-performance JPEG encoder for still image and video compression applications.

One of the fastest available JPEG encoders, the JPEG-E can encode at Full HD (1080p30) or higher rates, even in Cyclone-III devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E megafunction ideal for interoperable systems and devices. In addition to generating standalone Baseline JPEG streams, the megafunction is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. The JPEG-E can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the megafunction fits in a variety of Altera devices, requiring, for example, approximately 5,800 slices for a Cyclone-IV implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 280 MSamples/sec in a Startix-IV device.

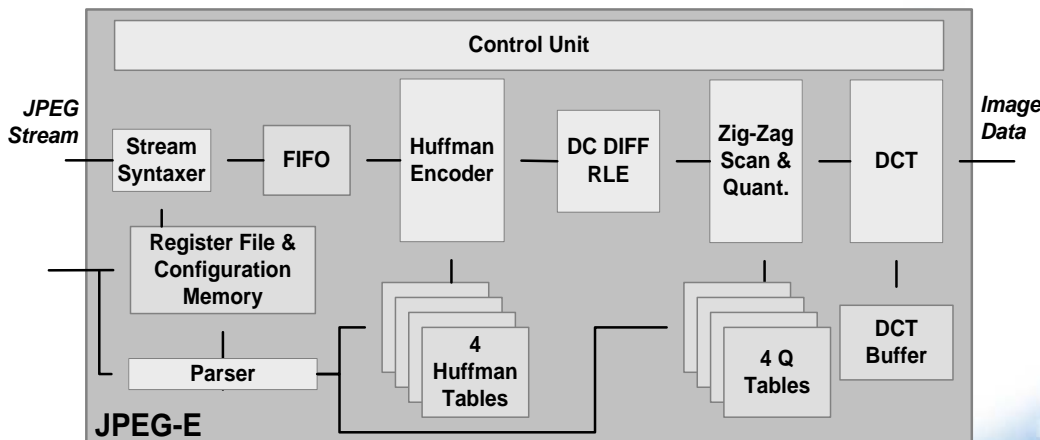
The megafunction is designed with easy to use, fully controllable and FIFO-like, Avalon Streaming input and output interfaces. Being carefully designed, rigorously verified and production-proven, the JPEG-E is a reliable and easy to integrate megafunction. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E megafunction is suitable for implementing a variety of digital imaging applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, scanners, etc)
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram



Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC)
- Programmable quantization tables (up to four)
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers
- Standalone, Baseline JPEG stream output

Additional Processing Capabilities

- Motion JPEG payload encoding
- Rate-Control (optional)

Designed for Easy Integration

- Simple and zero latency streaming interfaces
- Single clock per input sample processing rate
- Fully programmable through standard JPEG marker segments
- Automatic JPEG markers generation on the output
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Easily fits most Altera device families (see implementation results table)

Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The megafunction's configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are input to the JPEG-E in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-E can address the most demanding image and video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized..

Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following Altera results are obtained after speed optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

| Altera Device | Logic | Fmax (MHz) | Special Features | Quartus Version |
|-----------------------|-------------|------------|------------------------|-----------------|
| Cyclone-III EP3C10-6 | 5,858 LEs | 170 MHz | 7 M9K 18 DSP 9-bit | 9.1 |
| Cyclone-IV EP4CGX22-6 | 5,792 LEs | 170 MHz | 7 M9K 19 DSP 9-bit | 9.1 |
| Stratix-II EP2S15-3 | 5,172 ALUTs | 225 MHz | 9 M4K 18 DSP 9-bit | 9.1 |
| Stratix-III EP3SE50-2 | 4,994 ALUTs | 260 MHz | 7 M9K 15 DSP 18-bit | 9.1 |
| Stratix-IV EP4S40G2-2 | 4,903 ALUTs | 280 MHz | 7 M9K 15 DSP 18-bit | 9.1 |

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis VQM or QXP netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Meafunctions

- JPEG-E-X Baseline/Extended Sequential JPEG Encoder – adds support for 12 bits per sample
- SVE-JPEG-E SpeedView Enabled JPEG Encoder that produces SpeedView enabled JPEG data streams.
- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-E core.