

CAST

JPEG-E-X

Baseline/Extended Sequential JPEG Encoder Core

This IP core is a high-performance image encoder that complies with both the Baseline (8-bit) and Extended Sequential (12-bit) DCT modes of the ISO/IEC 10918-1 JPEG standard. The core's lossy image compression conforms to DICOM, the Digital Imaging and Communications in Medicine standard.

The core features a compact, fast design. For example, it can process 450 MSamples/sec with only 69K gates in a typical ASIC 0.09-micron process, or 280 MSamples/sec in high-end FPGA devices, or even 30 frames per second of 16:9 HDTV 1080p video in low-end FPGAs.

In addition to processing from 8- through 12-bit JPEG image streams, the core can also compress non-standard motion JPEG streams. It can be enhanced with an optional add-on bit-rate control block, which may benefit applications that have tight bandwidth constraints.

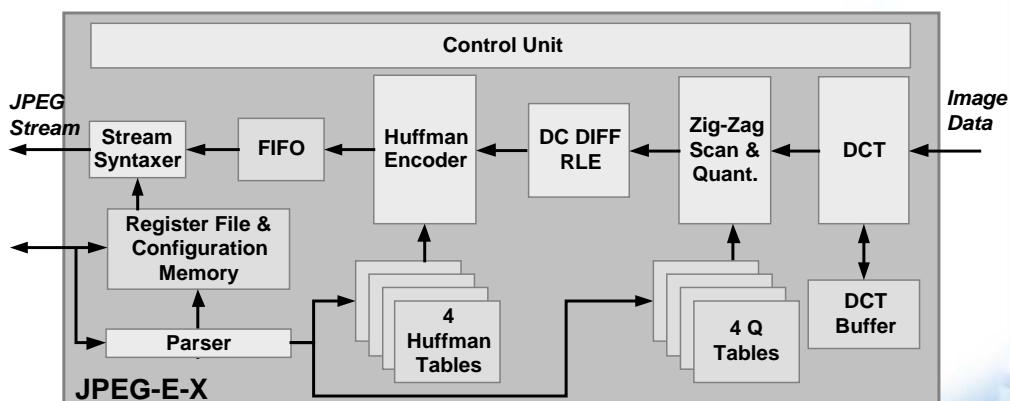
The core includes FIFO-like pixel and stream input/output interfaces. Other standard interfaces (e.g. AMBA) are available. The core is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance JPEG-E-X core is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline/Extended Sequential ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Compatible with the Digital Imaging and Communications in Medicine (DICOM) standard

Additional Image Processing Capabilities

- Motion JPEG encoding
- Rate-Control (optional)

Designed for Easy Integration

- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture

Functional Description

The core is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples (8 or 12 bit each) in any color space format are input to the JPEG-E-X in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the JPEG-E-X can address the most demanding frame-based video compression applications. The JPEG-E-X outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

Implementation Results

JPEG-E-X reference designs have been evaluated in a variety of technologies. The following ASIC results are sample pre-layout ASIC results (as reported by the synthesis tool and silicon vendor design kit under typical conditions), with all core I/Os assumed to be routed on-chip.

ASIC Technology	Frequency	Logic Area ¹	Number of Eq. Gates ²	Memory (bits)
UMC 0.18μ	250 MHz	819,428	82,113	23,680
TSMC 0.09μ	450 MHz	194,600	68,948	23,680

¹ Excluding memory

² Equivalent gates count uses the smallest NAND2 gate available in the technology

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001).
- Simulation script, vectors, expected results, and comparison utility.
- Software (C++) Bit-Accurate Model
- Synthesis script.
- Comprehensive user documentation, including detailed specifications and a system integration guide.