JPEG-E-X
Baseline & Extended JPEG Encoder Core

Implements a high-performance image encoder that complies with both the Baseline (8-bit) and Extended Sequential (12-bit) DCT modes of the ISO/IEC 10918-1 JPEG standard.

One of the fastest available Extended JPEG encoders, the JPEG-E-X can encode at Full HD (1080p30) or higher rates, even in FPGA devices. Full compliance with the Baseline and the Extended Sequential DCT modes of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E-X core ideal for interoperable systems and devices such as consumer digital cameras, camcorders, office automation equipment, medical imaging systems, video conference systems and remote surveillance systems.

The produced JPEG streams conform also to the Digital Imaging and Communications in Medicine (DICOM) requirements. In addition to generating standalone Baseline or Extended JPEG streams, the core is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. Furthermore, bandwidth-constraint applications may benefit from the included programmable bit-rate control block.

The core includes FIFO-like pixel and stream input/output interfaces. Other standard interfaces (e.g. AMBA) are available. The core is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a complete verification environment and software bit-accurate model.

Applications
The high-performance JPEG-E-X core is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems
- Portable multimedia devices (smart-phones, tablets, PDAs etc)

Features

Baseline & Extended ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components
- All possible scan configurations and all JPEG formats for input/output data
- Image size up to 64k x 64k
- DNL and restart markers

Additional Processing Capabilities

- Programmable Quantization Quality (1 to 100)
- Motion JPEG encoding
- Digital Imaging Communication in Medicine (DICOM) standard conformance
- One-pass compression ratio regulation (optional)
  - Motion JPEG video oriented rate control option with programmable nominal output frame size and transmission buffer size in bytes
  - Block-based, rate control option with independent Luminance and Chrominance thresholds

Designed for Easy Integration

- Simple, microcontroller like, programming interface
- Avalon-ST™ I/O data interfaces
- Optional AHB or AXI bus interfaces
- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture
Functional Description

The core is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples (8 or 12 bit each) in any color space format are input to the JPEG-E-X in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the JPEG-E-X can address the most demanding frame-based video compression applications. The JPEG-E-X outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

Implementation Results

JPEG-E-X reference designs have been evaluated in a variety of technologies. The following ASIC results are sample pre-layout ASIC results (as reported by the synthesis tool and silicon vendor design kit under typical conditions), with all core I/Os assumed to be routed on-chip.

<table>
<thead>
<tr>
<th>ASIC Technology</th>
<th>Frequency (MHz)</th>
<th>Logic Area (um²)</th>
<th>Number of Eq. Gates</th>
<th>Memory (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMC 0.18µ</td>
<td>250</td>
<td>819,428</td>
<td>82,113</td>
<td>23,680</td>
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<tr>
<td>TSMC 0.09µ</td>
<td>450</td>
<td>194,600</td>
<td>68,948</td>
<td>23,680</td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- Simulation script, vectors, expected results, and comparison utility.
- Software (C++) Bit-Accurate Model
- Synthesis script.
- Comprehensive user documentation, including detailed specifications and a system integration guide.