

CAST



JPEG-E-X

Baseline & Extended JPEG Encoder Core

The JPEG-E-X core is a standalone and high-performance 8-bit and 12-bit JPEG encoder for still image and video compression applications.

One of the fastest available Extended JPEG encoders, the JPEG-E-X can encode at Full HD (1080p30) or higher rates, even in FPGA devices. Full compliance with the Baseline and the Extended Sequential DCT modes of the ISO/IEC 10918-1 JPEG standard makes the JPEG-E-X core ideal for interoperable systems and devices. The produced JPEG streams conform also to the Digital Imaging and Communications in Medicine (DICOM) requirements. In addition to generating standalone Baseline or Extended JPEG streams, the core is also capable of producing the (de facto) standard video payload of many motion JPEG container formats. The JPEG-E-X can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the core fits in a variety of Xilinx devices, requiring, for example, approximately 1,400 slices for a Spartan-6 implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 250 MSamples/sec in a Virtex-6 device.

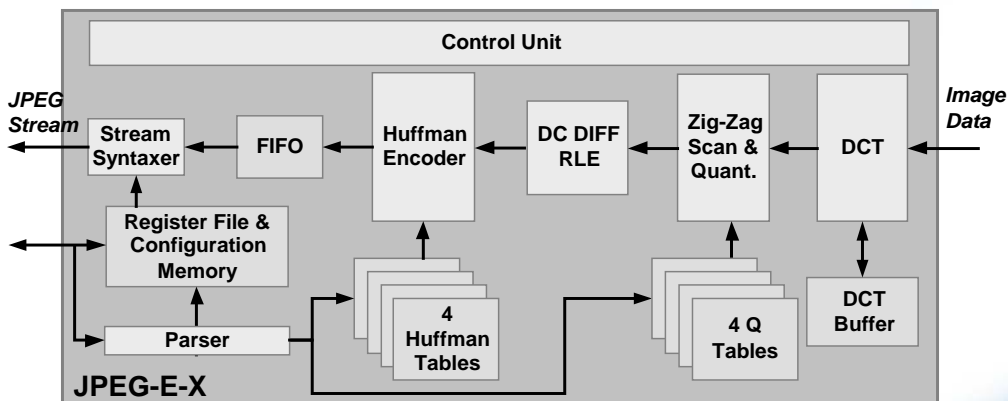
The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed and rigorously verified, the JPEG-E-X is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E-X core is suitable for implementing a variety of digital imaging applications, including:

- Medical imaging systems
- Digital cameras and camcorders
- Office automation and digital photo equipment (multi-function printers, scanners etc)
- Infrared imaging devices

Block Diagram



Features

Baseline & Extended ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC)
- Programmable quantization tables (up to four)
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers
- Standalone, Baseline or Extended JPEG stream output

Additional Processing Capabilities

- DICOM JPEG conformance
- Motion JPEG payload encoding
- Rate-Control (optional)

Designed for Easy Integration

- Simple and zero latency streaming interfaces
- Single clock per input sample processing rate
- Fully programmable through standard JPEG marker segments
- Automatic JPEG markers generation on the output
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- Easily fits most Xilinx device families (see implementation results table)

Functional Description

The JPEG-E-X is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The core's configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are input to the JPEG-E-X in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-E-X can address the most demanding image and video compression applications. The JPEG-E-X outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized.

Implementation Results

JPEG-E-X reference designs have been evaluated in a variety of technologies. The following Xilinx results are obtained after area optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

Xilinx Device	Slices	Fmax (MHz)	I/O	BRAM	Special Features	ISE
Spartan-3 3S1000-5	2,855	105	84	7 RAMB16	9 MULT18	12.2
Spartan-6 6SLX9-3	1,427	170	84	7 RAMB16	9 DSP48	12.2
Virtex-5 5VLX30-3	1,291	225	84	1 RAMB36 3 RAMB18	9 DSP48	12.2
Virtex-6 6VLX75T-3	1,767	250	84	1 RAMB36 5 RAMB18	9 DSP48	12.2

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide