



JPEG-E-X

Baseline/Extended Sequential JPEG Encoder Megafunction

This IP megafunction is a high-performance image encoder that complies with both the Baseline (8-bit) and Extended Sequential (12-bit) DCT modes of the ISO/IEC 10918-1 JPEG standard. The megafunction's lossy image compression conforms to DICOM, the Digital Imaging and Communications in Medicine standard.

The megafunction features a compact, fast design. For example, it can process 450 MSamples/sec with only 69K gates in a typical ASIC 0.09-micron process, or 280 MSamples/sec in high-end FPGA devices, or even 30 frames per second of 16:9 HDTV 1080p video in low-end FPGAs.

In addition to processing from 8- through 12-bit JPEG image streams, the megafunction can also compress non-standard motion JPEG streams. It can be enhanced with an optional add-on bit-rate control block, which may benefit applications that have tight bandwidth constraints.

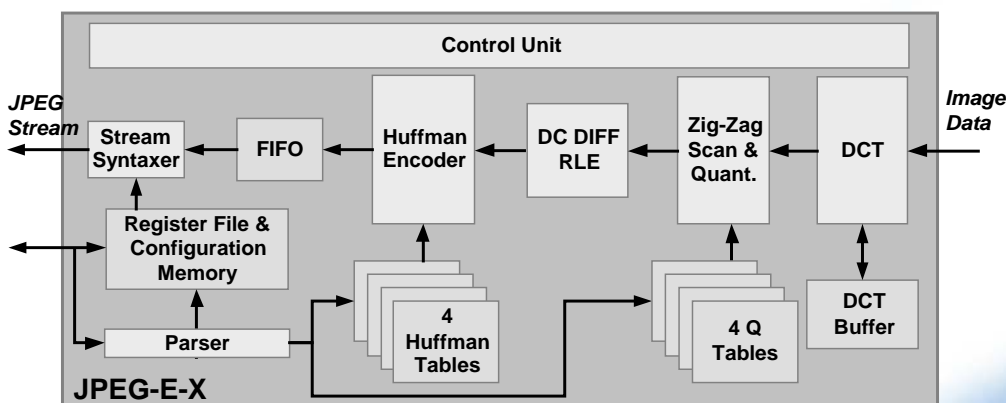
The megafunction includes FIFO-like pixel and stream input/output interfaces. Other standard interfaces (e.g. AMBA) are available. The megafunction is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance JPEG-E-X megafunction is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline/Extended Sequential ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Compatible with the Digital Imaging and Communications in Medicine (DICOM) standard

Additional Image Processing Capabilities

- Motion JPEG encoding
- Rate-Control (optional)

Designed for Easy Integration

- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture
- Easily fits most Altera device families (see implementation table)

Functional Description

The megafunction is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The megafunction's configuration can be modified after the encoding of one or multiple frames. Image samples (8 or 12 bit each) in any color space format are input to the JPEG-E-X in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the JPEG-E-X can address the most demanding frame-based video compression applications. The JPEG-E-X outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

Implementation Results

JPEG-E-X reference designs have been evaluated in a variety of technologies. The following Altera results are obtained after area optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

Altera Device	Logic	Frequency	Special Features	Quartus Version
Cyclone-III EP3C10-6	6,899 LEs	170 MHz	8 M9K 18 DSP 9-bit	9.1
Cyclone-IV EP4CGX22-6	6,817 LEs	170 MHz	8 M9K 18 DSP 9-bit	9.1
Stratix-II EP2S15-3	6,140 ALUTs	225 MHz	10 M4K 18 DSP 9-bit	9.1
Stratix-III EP3SE50-2	5,875 ALUTs	260 MHz	8 M9K 18 DSP 18-bit	9.1
Stratix-IV EP4S40G2-2	5,796 ALUTs	280 MHz	8 M9K 18 DSP 18-bit	9.1

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA technologies.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors, expected results, and comparison utility
- Software (C++) Bit-Accurate Model
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide