

CAST

JPEG-D

Baseline JPEG Decoder Core

Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Up to four Huffman Tables (two DC, two AC)
- Up to four quantization tables
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers

Additional Processing Capabilities

- Motion JPEG payload decoding

Designed for Easy Integration

- Standalone operation
- Automatic self-programming by JPEG markers parsing
- Marker errors catching
- Broadcasting of decoded image parameters for controlling peripherals such as a block-to-raster scan converter

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs

The JPEG-D core is a standalone and high-performance JPEG decoder for still image and video decompression applications.

One of the fastest available JPEG decoders, the JPEG-D can decode multiple Full HD channels, even in FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-D core ideal for interoperable systems and devices. In addition to decoding standard Baseline JPEG streams, the core is also capable of decompressing the video payload of many (de facto) standard motion JPEG container formats.

Evaluation designs show that the core has a small footprint, requiring, for example, approximately 61,000 equivalent gates and 14kbits of internal memory for a 90nm implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 450 MSamples/sec in a 90nm technology.

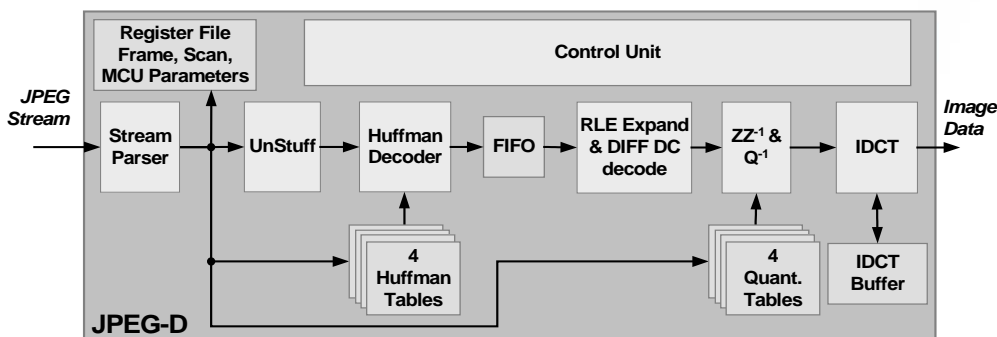
The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and production-proven, the JPEG-D is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-D core is suitable for implementing a variety of digital imaging applications, including:

- Home entertainment devices (set-top boxes, network media players etc)
- Portable multimedia devices (media players, mobile phones etc)
- Digital printing devices
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram



Functional Description

The JPEG-D is fully self-configured by parsing the marker segments that are present in the input Baseline JPEG stream. The core checks also the input JPEG marker segments against errors and signals in case it detects any. The decoded image parameters are made available for controlling peripherals such as a block-to-raster scan converter.

Following the parsing of the marker segments, the JPEG-D decodes the entropy coded data segment(s) and outputs the decoded image samples in their native MCU block scan order.

Designed for continuous data flow, the JPEG-D can address the most demanding image and video decompression applications..

Implementation Results

JPEG-D reference designs have been evaluated in a variety of technologies. The following are sample pre-layout ASIC results (as reported by the synthesis tool and silicon vendor design kit under typical conditions) optimized for speed.

ASIC Technology	Logic Eq. Gates	Fmax (MHz)	Memory
UMC 0.18 μ process	68,459	300 MHz	14,400 bits
TSMC 0.09 μ process	61,061	450 MHz	14,400 bits

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Synthesis script.
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Cores

- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-D core.